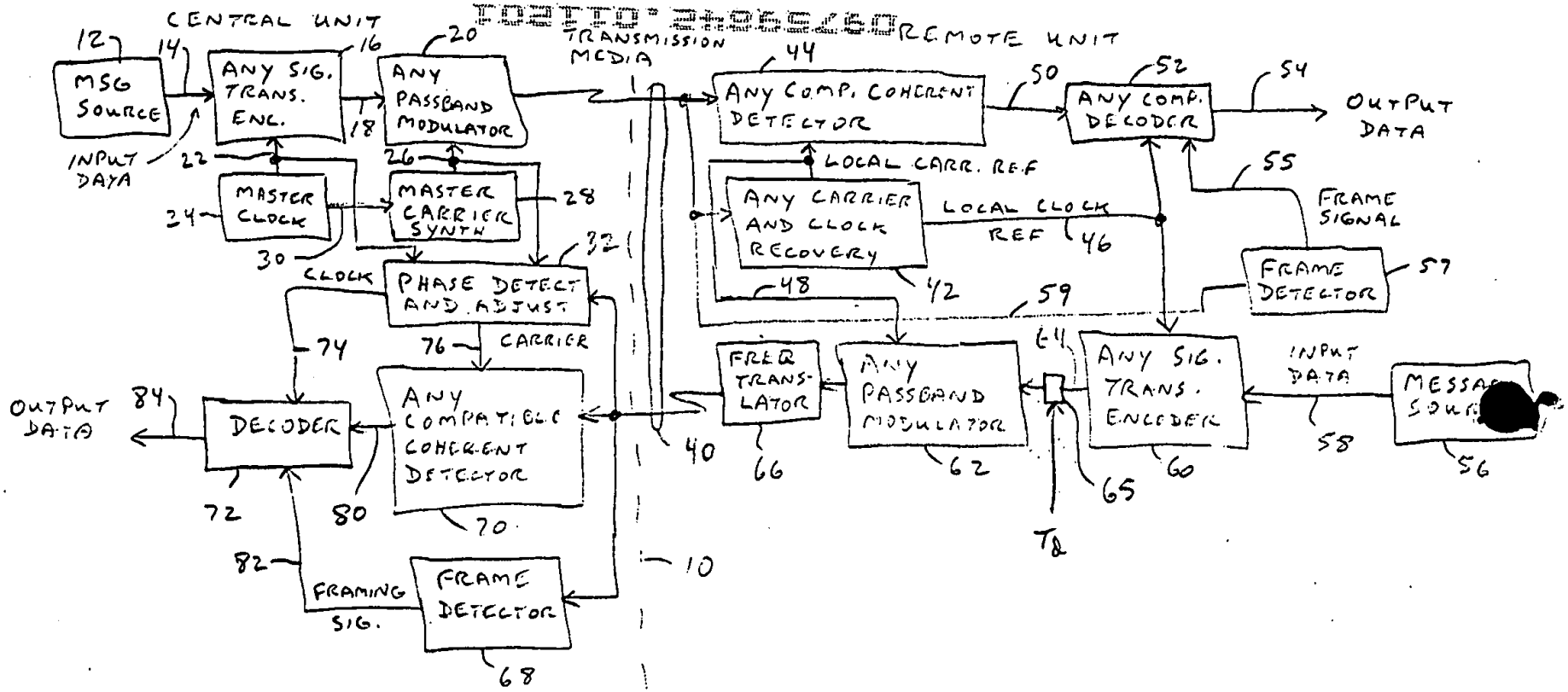
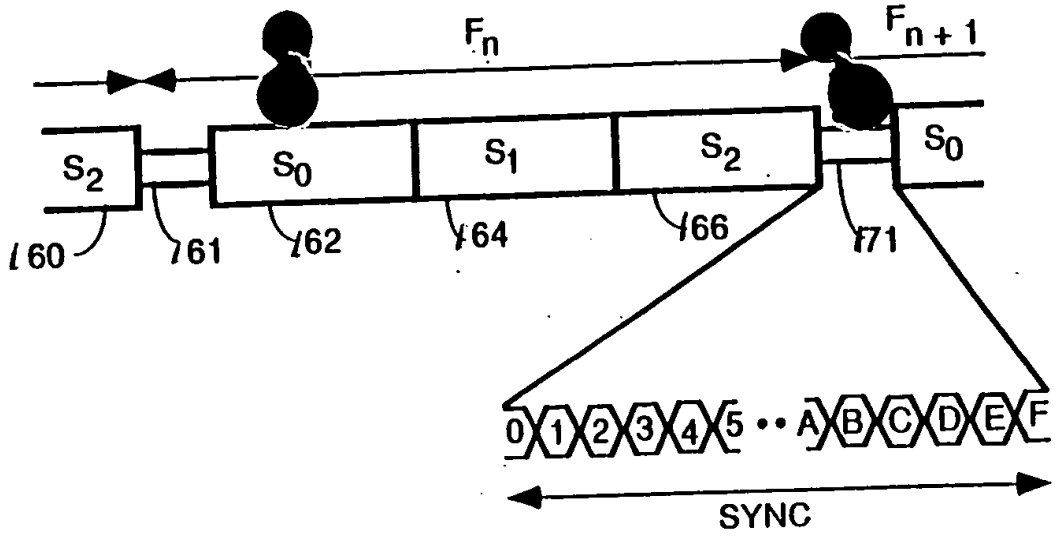
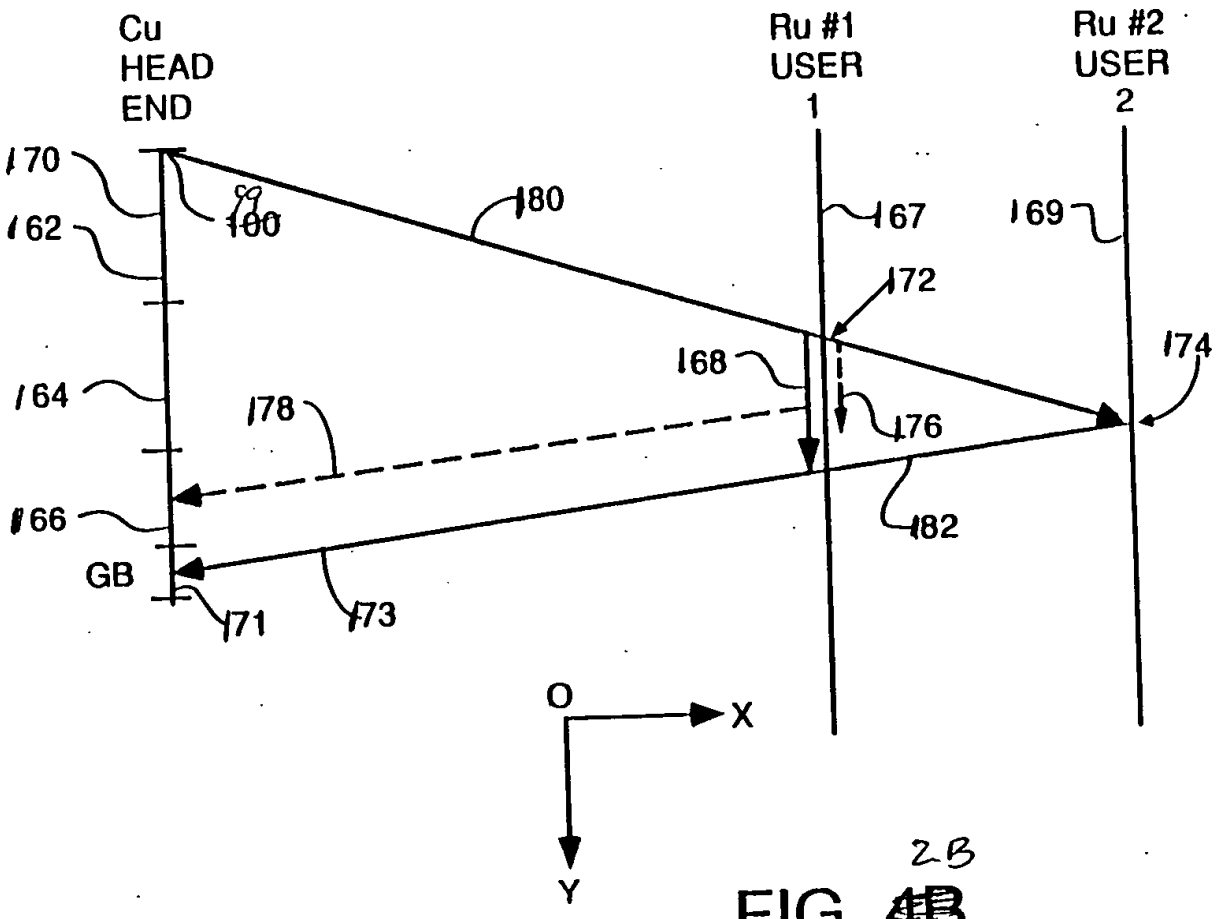

CENTRAL UNIT
REMOTE UNIT
TRANSMISSION MEDIA
MSG SOURCE
ANY SIG. TRANS. ENC.
ANY PASSBAND MODULATOR
INPUT DATA
MASTER CLOCK
MASTER CARRIER SYNTH
PHASE DETECT AND ADJUST
CLOCK
CARRIER
DECODER
OUTPUT DATA
ANY COMPATIBLE COHERENT DETECTOR
FRAMING SIG.
FRAME DETECTOR
ANY COMP. COHERENT DETECTOR
LOCAL CARR. REF
ANY CARRIER AND CLOCK RECOVERY
LOCAL CLOCK REF
ANY COMP. DECODER
OUTPUT DATA
FRAME SIGNAL
FRAME DETECTOR
FREQ TRANS-LATOR
ANY PASSBAND MODULATOR
ANY SIG. TRANS. ENCODER
INPUT DATA
MESSAGE SOURCE
12
14
16
18
20
22
24
26
28
30
32
40
42
44
46
48
50
52
54
55
56
57
58
59
60
62
64
65
66
68
70
72
74
76
80
82
84
10
T_d

FIG. 1



2A

FIG. 4A



2B

FIG. 4B

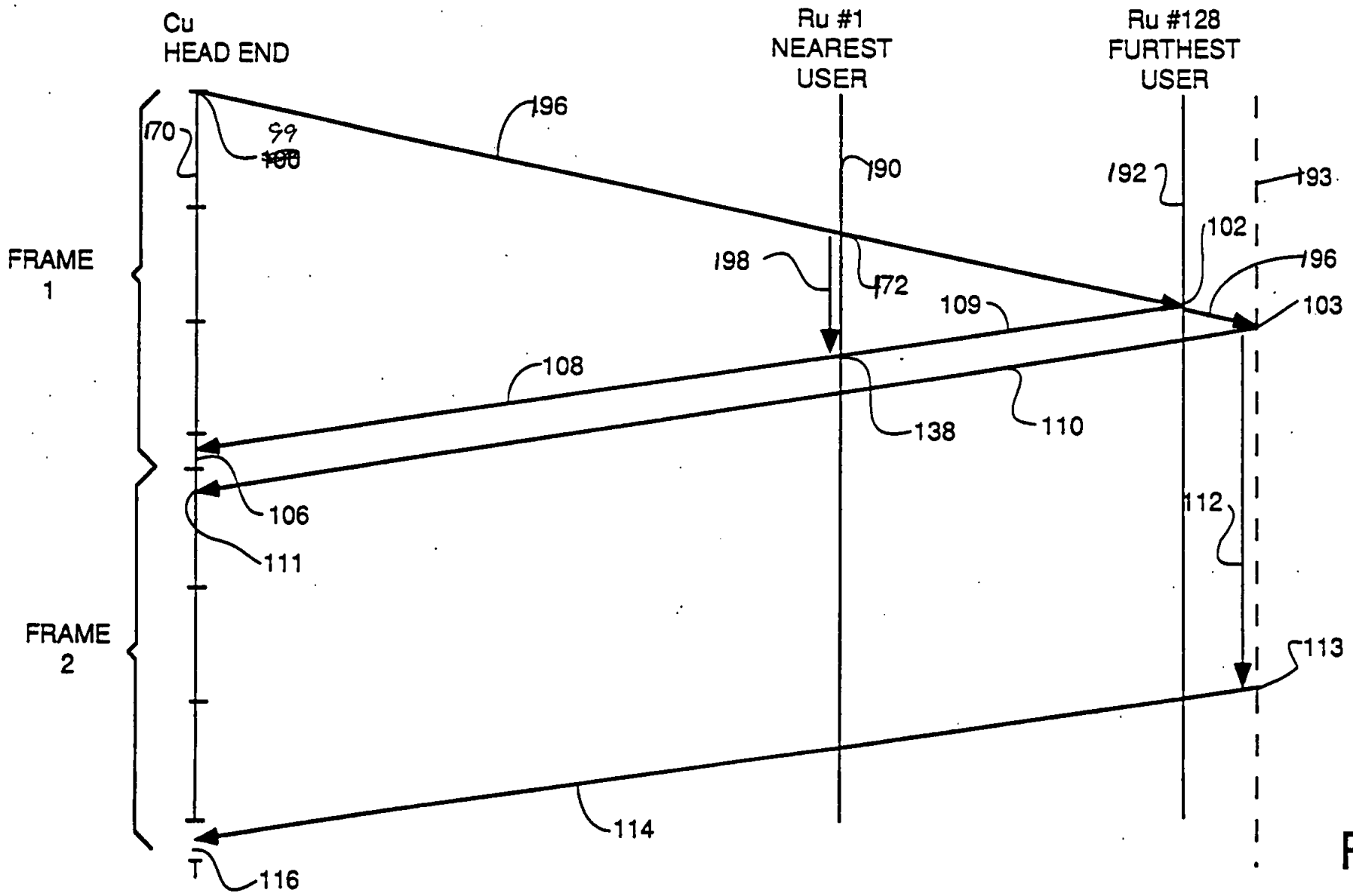


FIG. 3

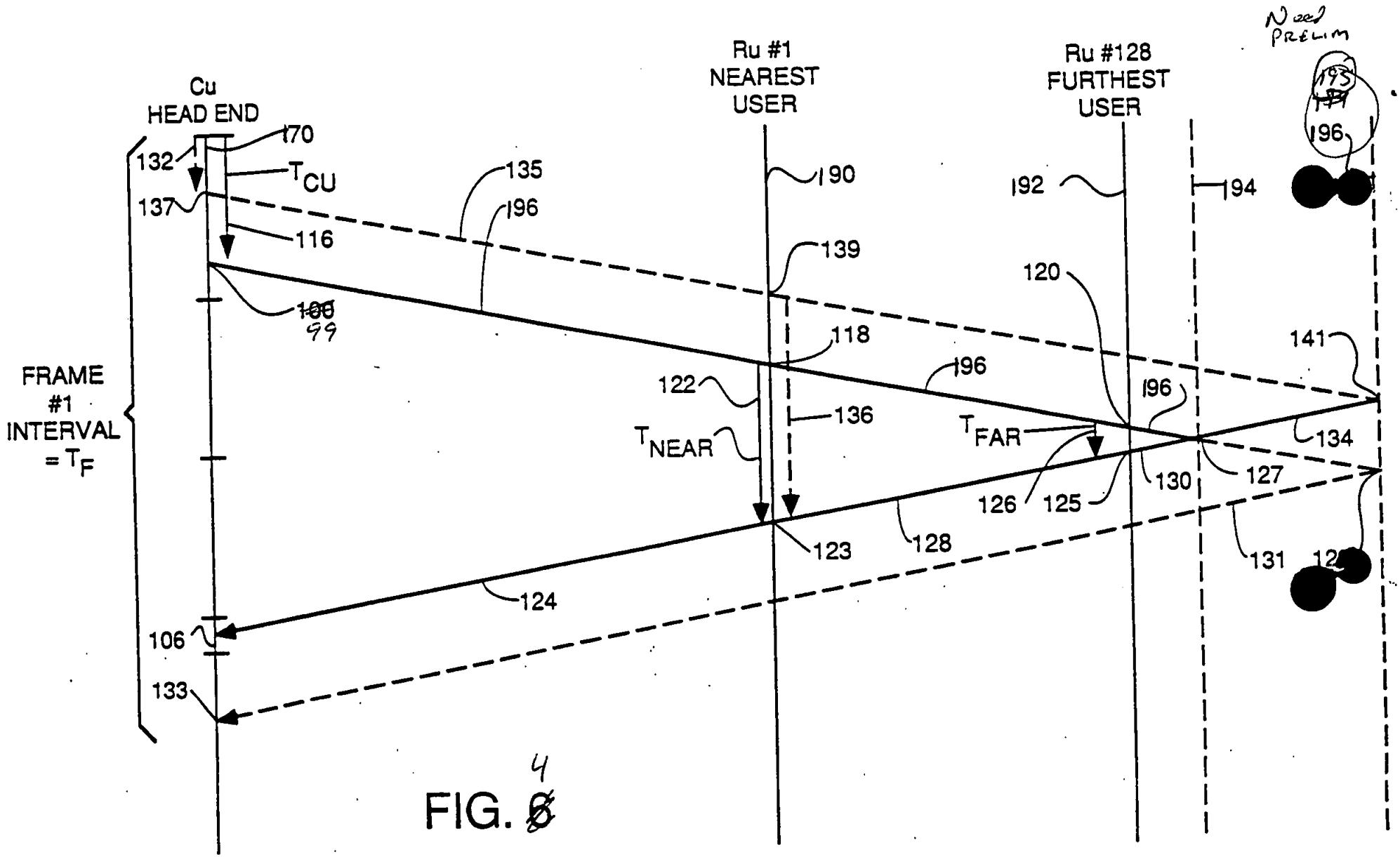
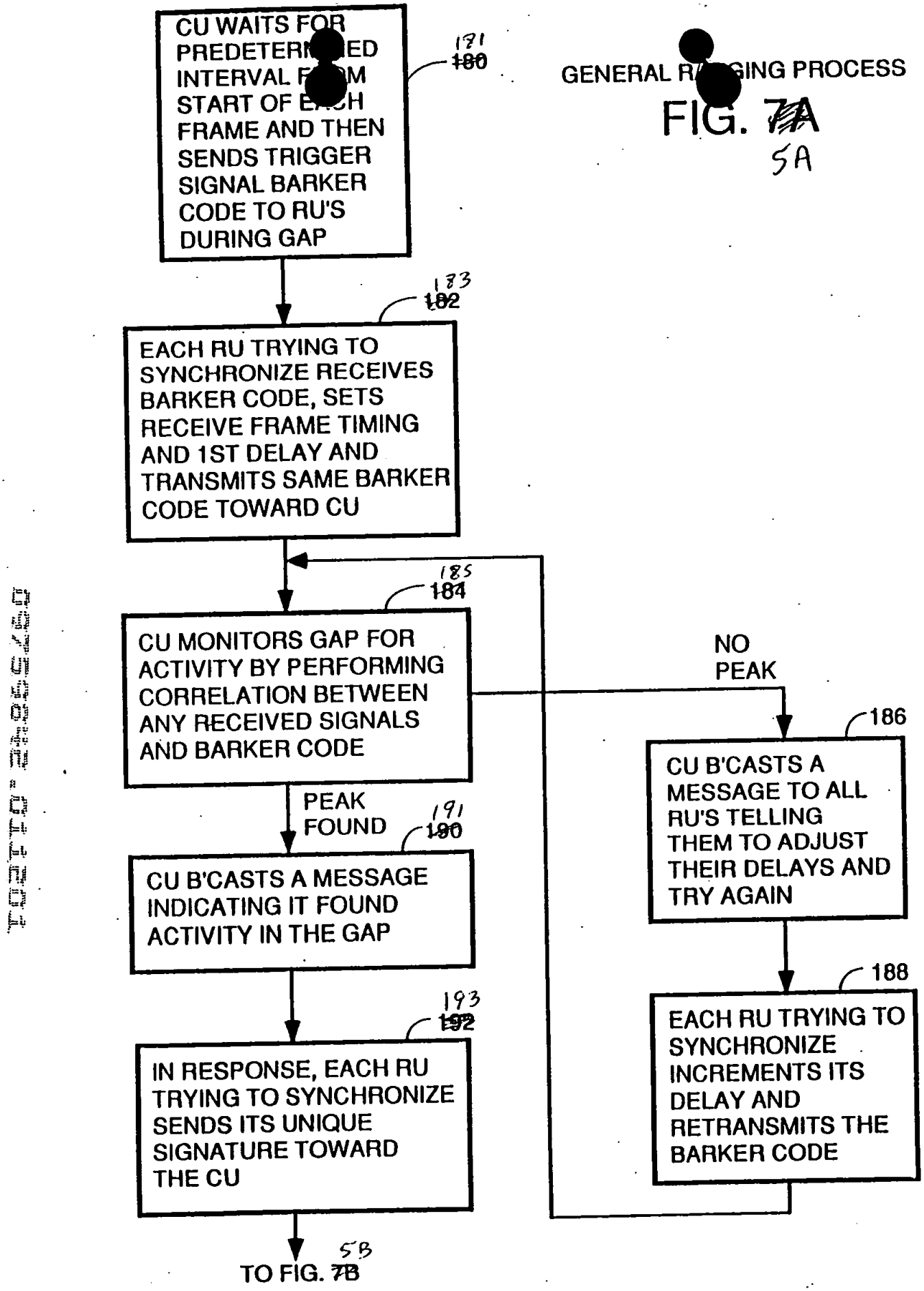
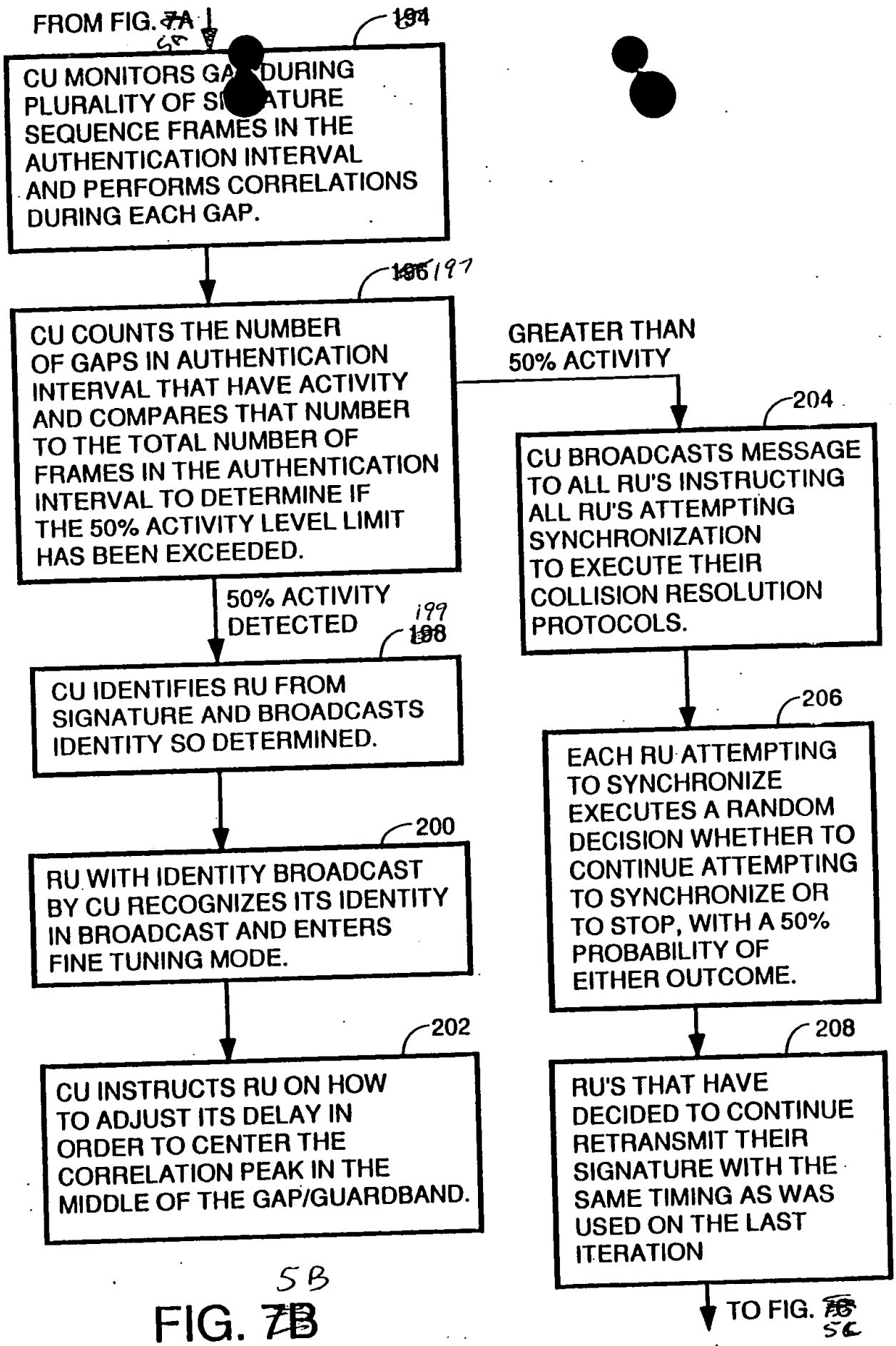


FIG. 4


GENERAL RANGING PROCESS
FIG. 7A
5A
CU WAITS FOR PREDETERMINED INTERVAL FROM START OF EACH FRAME AND THEN SENDS TRIGGER SIGNAL BARKER CODE TO RU'S DURING GAP
180
181
EACH RU TRYING TO SYNCHRONIZE RECEIVES BARKER CODE, SETS RECEIVE FRAME TIMING AND 1ST DELAY AND TRANSMITS SAME BARKER CODE TOWARD CU
182
183
CU MONITORS GAP FOR ACTIVITY BY PERFORMING CORRELATION BETWEEN ANY RECEIVED SIGNALS AND BARKER CODE
184
185
NO PEAK
CU B'CASTS A MESSAGE TO ALL RU'S TELLING THEM TO ADJUST THEIR DELAYS AND TRY AGAIN
186
EACH RU TRYING TO SYNCHRONIZE INCREMENTS ITS DELAY AND RETRANSMITS THE BARKER CODE
188
PEAK FOUND
CU B'CASTS A MESSAGE INDICATING IT FOUND ACTIVITY IN THE GAP
190
191
IN RESPONSE, EACH RU TRYING TO SYNCHRONIZE SENDS ITS UNIQUE SIGNATURE TOWARD THE CU
192
193
TO FIG. 7B
5B


FROM FIG. 7A
5A
194
CU MONITORS GAPS DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
196/197
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
GREATER THAN 50% ACTIVITY
204
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
50% ACTIVITY DETECTED
199
198
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
206
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
200
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
202
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.
208
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. 7B
5C

5B

FIG. 7B

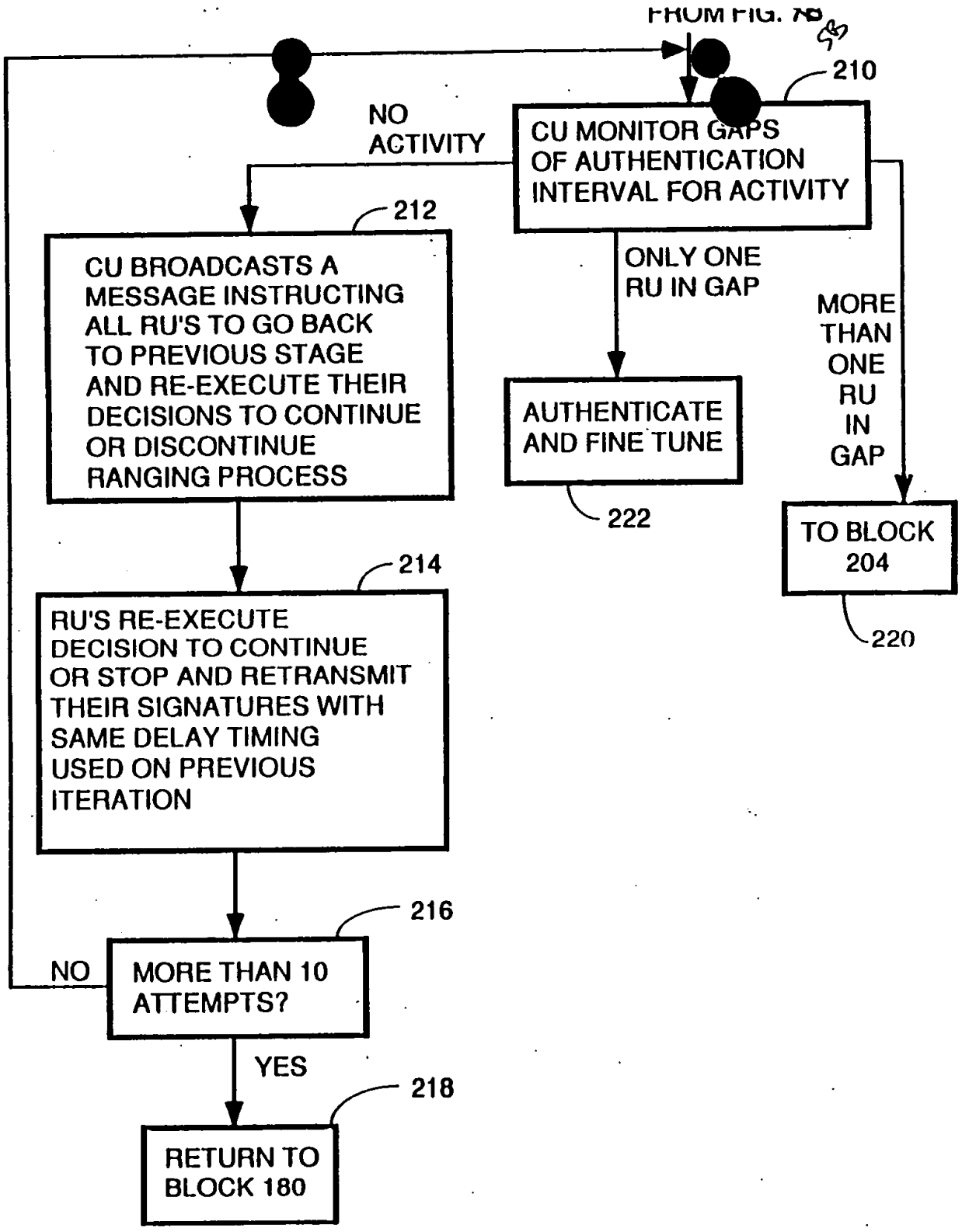
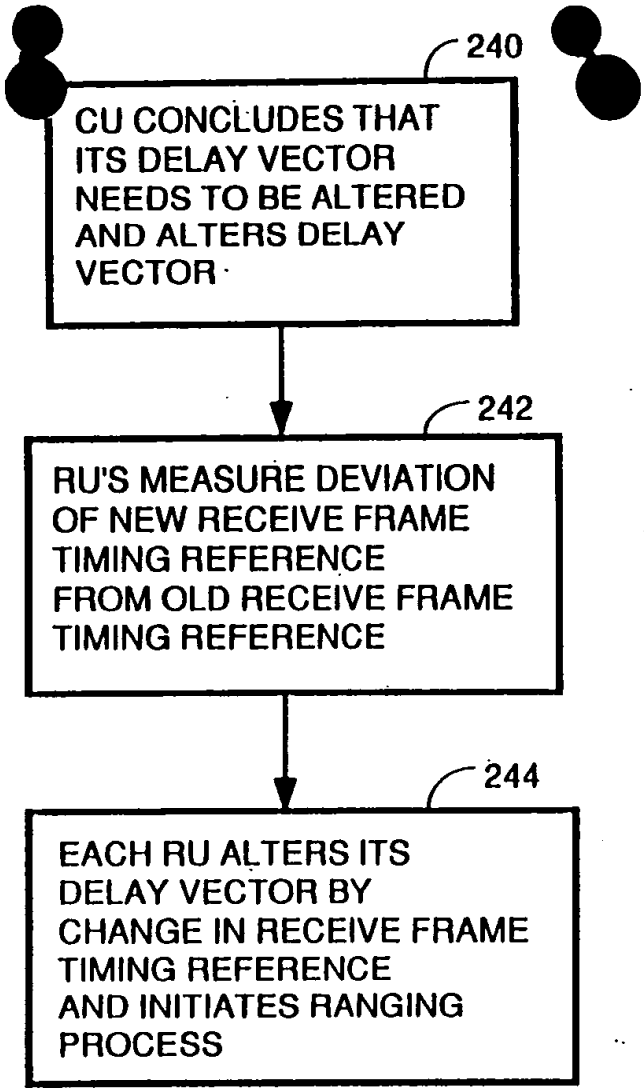

FROM FIG. 5B
210
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
NO ACTIVITY
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
ONLY ONE RU IN GAP
AUTHENTICATE AND FINE TUNE
222
MORE THAN ONE RU IN GAP
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. 5C ~~7C~~



6

FIG. 8

DEAD RECKONING RE-SYNC

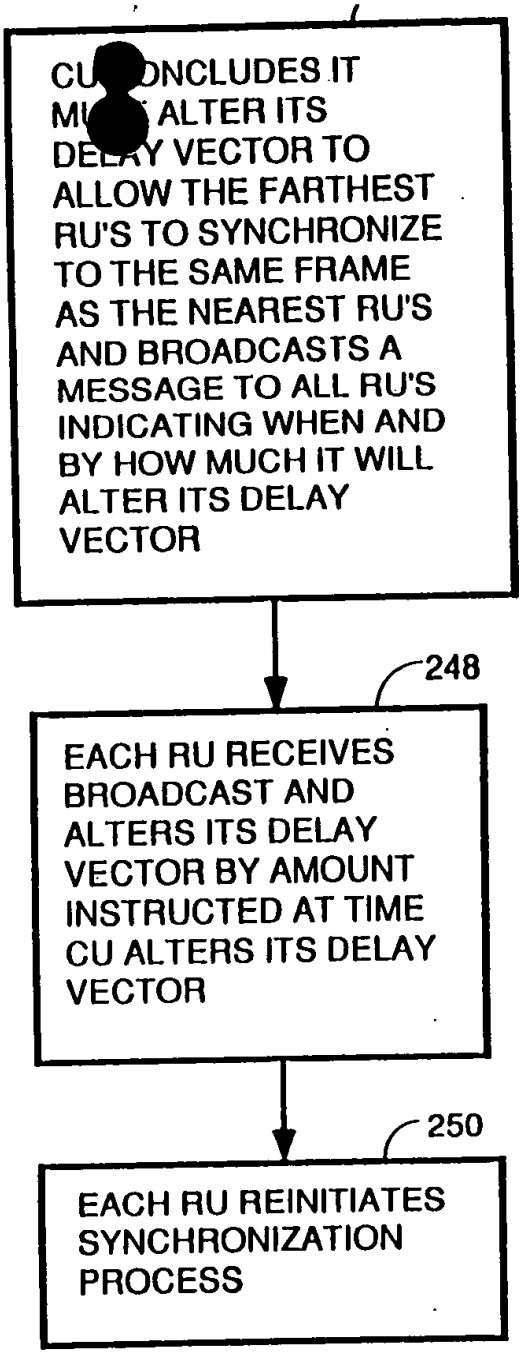
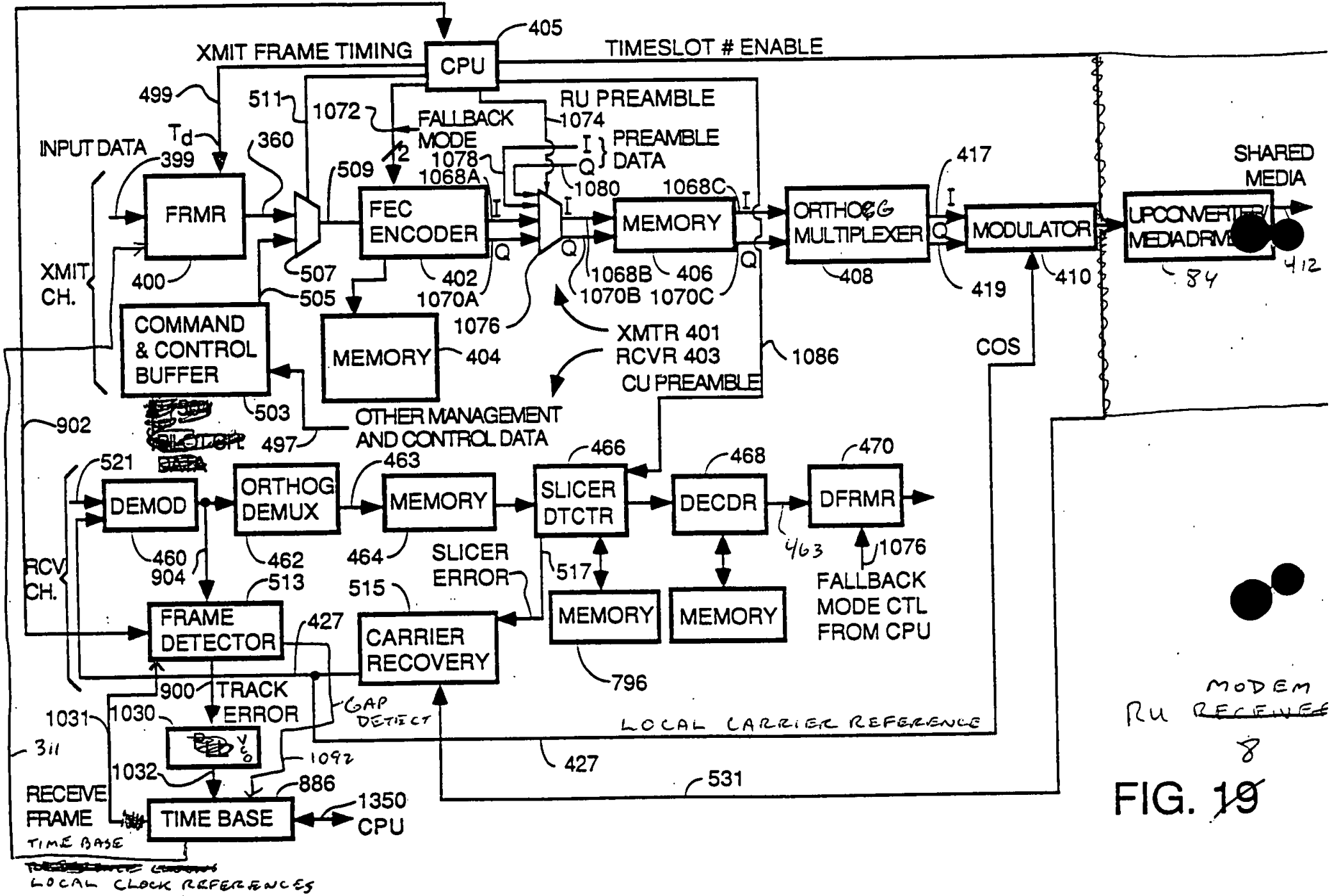


FIG. 9

PRECURSOR EMBODIMENT

RU

DIGITAL MODEM BLOCK DIAGRAM



MODEM RU RECEIVE

8

FIG. 19

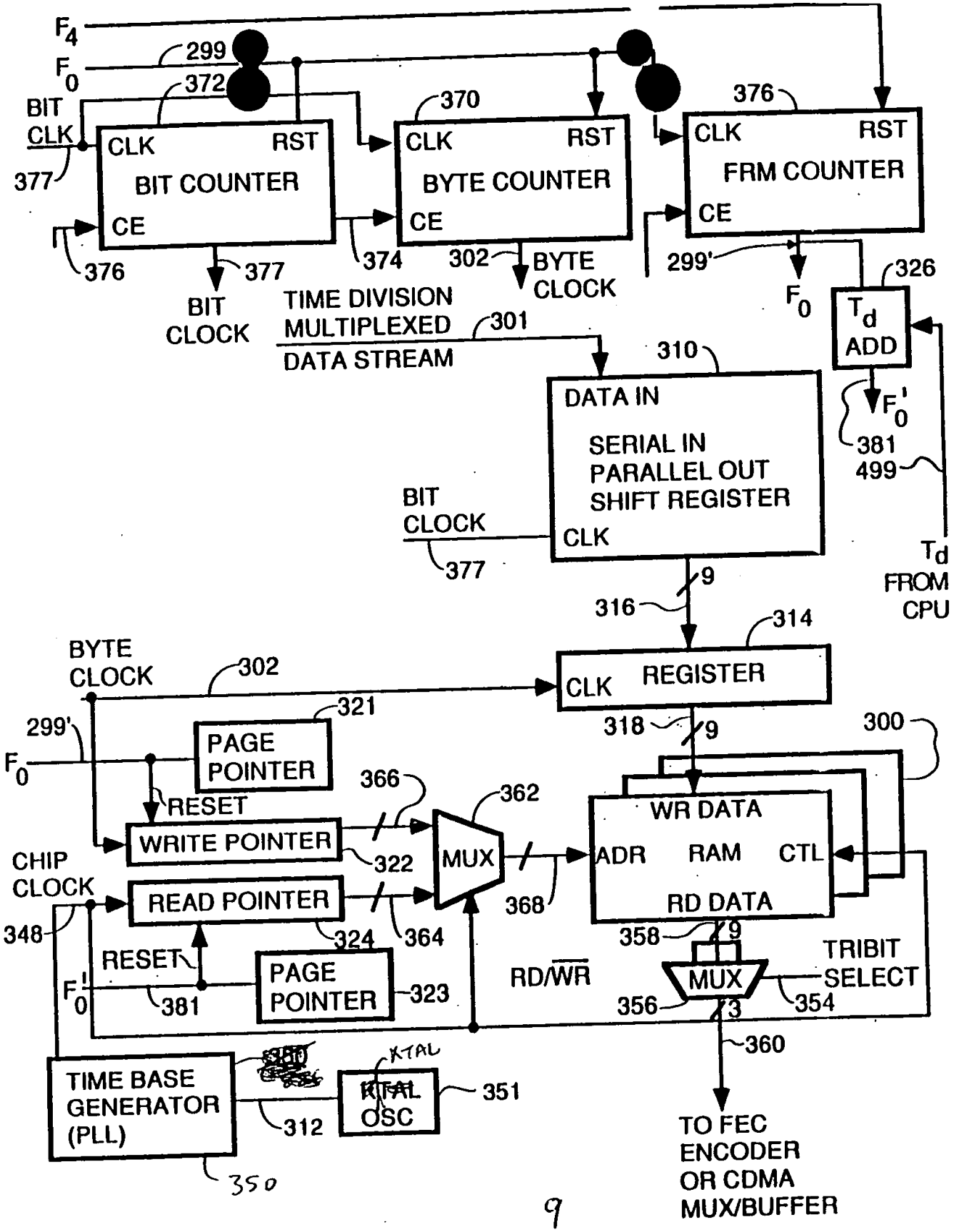

F4
F0
299
372
370
376
BIT CLK
377
CLK RST
BIT COUNTER
CE
CLK RST
BYTE COUNTER
CE
CLK RST
FRM COUNTER
CE
376
377
374
302
BYTE CLOCK
299'
F0
326
Td ADD
BIT CLOCK
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
CLK
F'0
381
499
BIT CLOCK
377
Td FROM CPU
9
316
314
BYTE CLOCK
302
CLK REGISTER
321
299'
318
9
300
F0
PAGE POINTER
366
362
RESET
WRITE POINTER
322
MUX
WR DATA
ADR RAM CTL
RD DATA
CHIP CLOCK
348
READ POINTER
324
364
368
358
9
TRIBIT SELECT
RESET
F'0
381
PAGE POINTER
323
RD/WR
MUX
356
3
354
360
TIME BASE GENERATOR (PLL)
312
XTAL OSC
351
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. 12

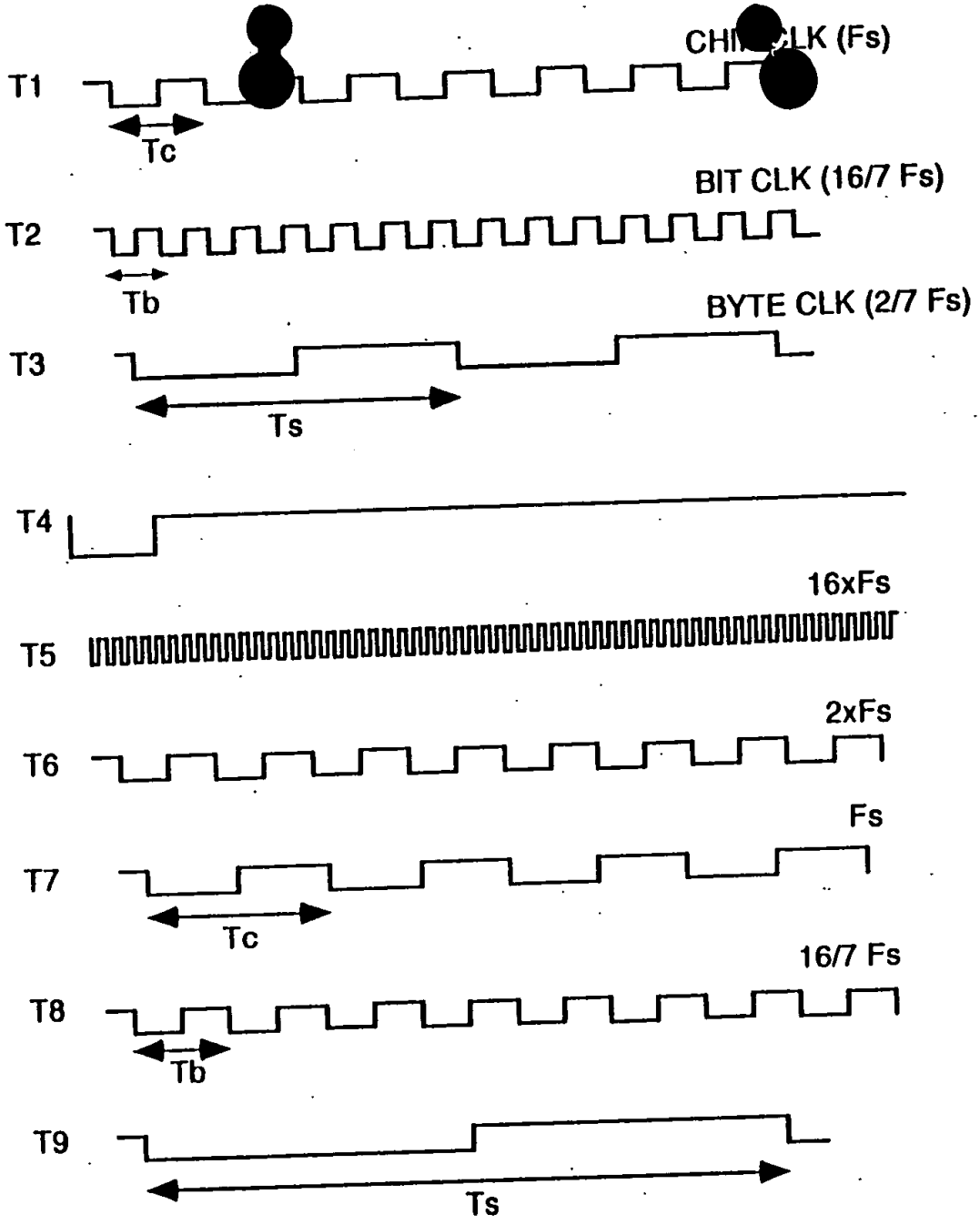
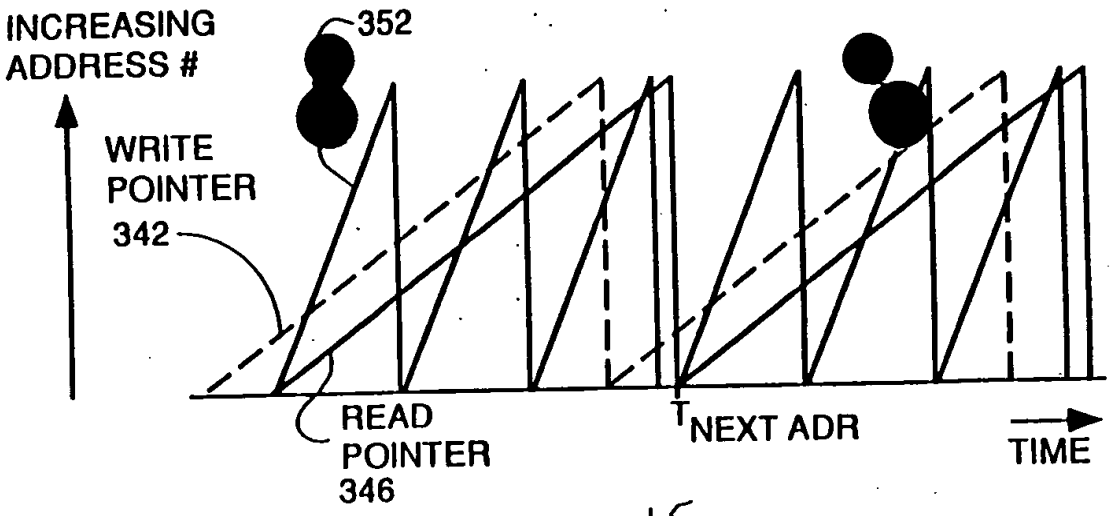
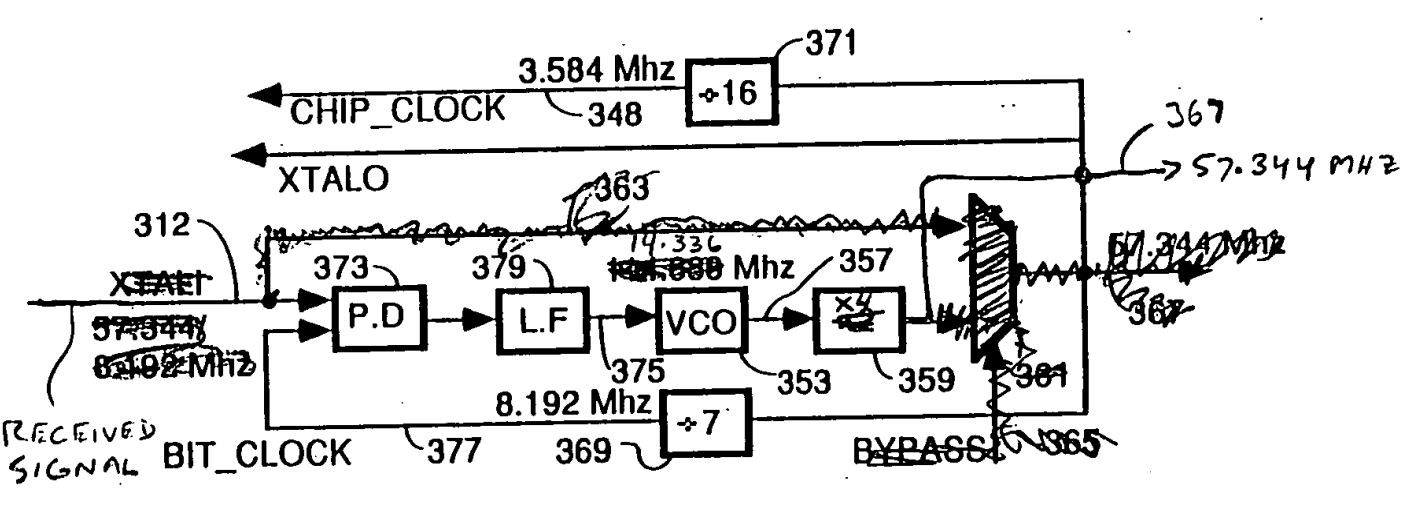

CHI CLK (Fs)
T1
Tc
BIT CLK (16/7 Fs)
T2
Tb
BYTE CLK (2/7 Fs)
T3
Ts
T4
16xFs
T5
2xFs
T6
Fs
T7
Tc
16/7 Fs
T8
Tb
T9
Ts

FIG. 10/13



15

FIG. 17



11

FIG. 18

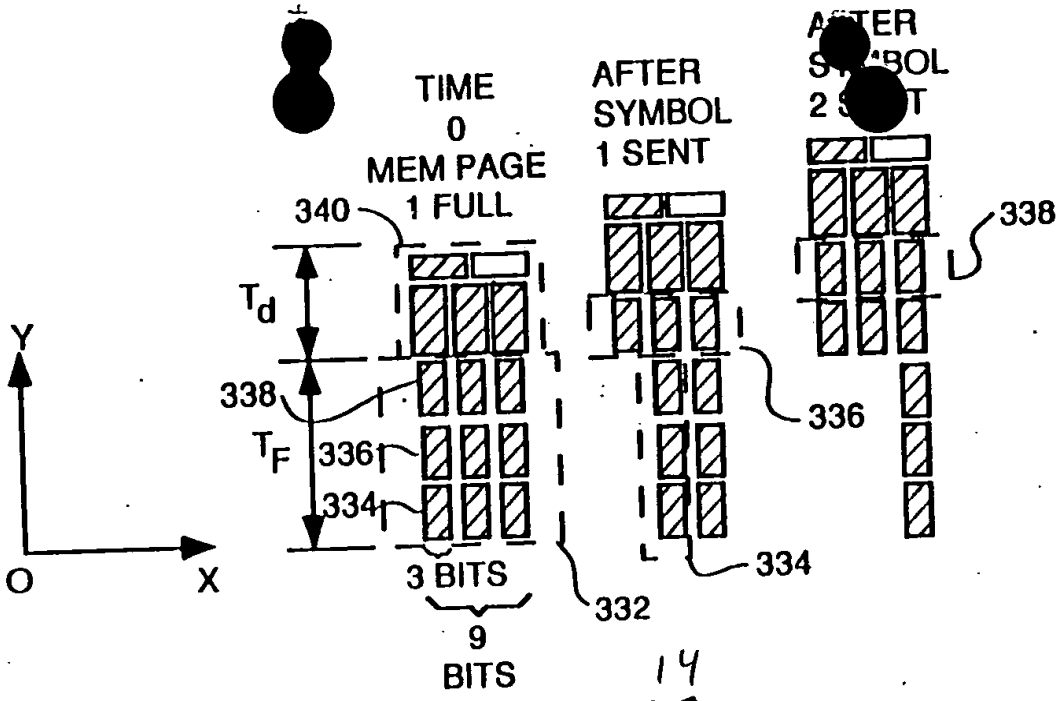


FIG. 14

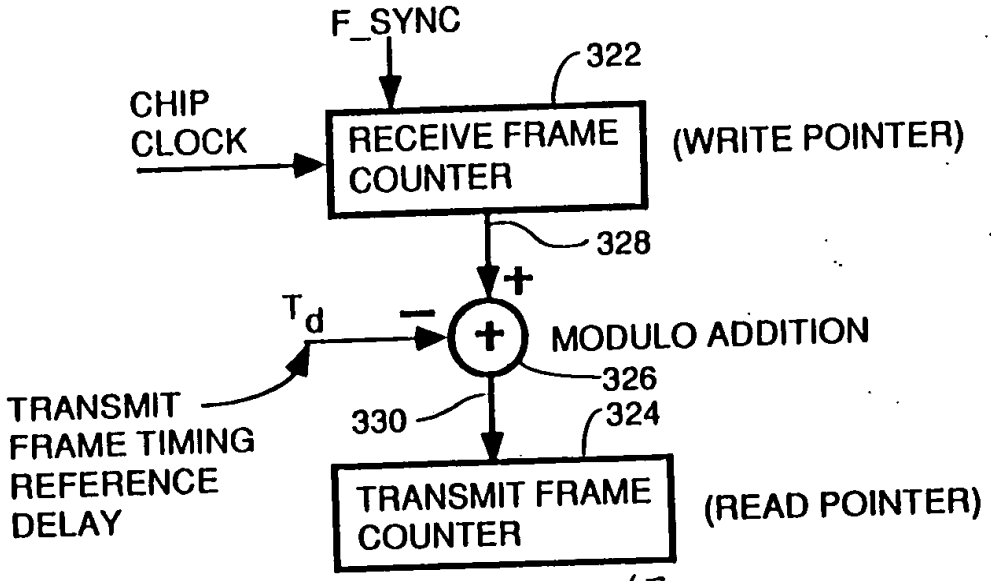


FIG. 15

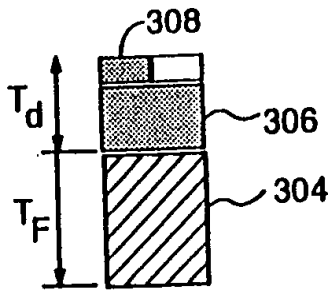


FIG. 16

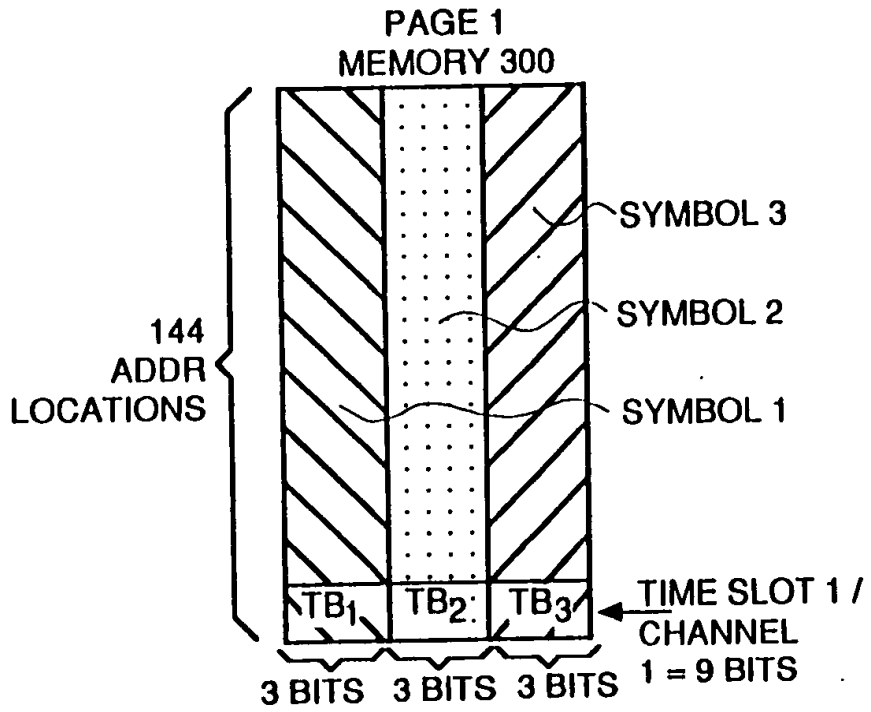
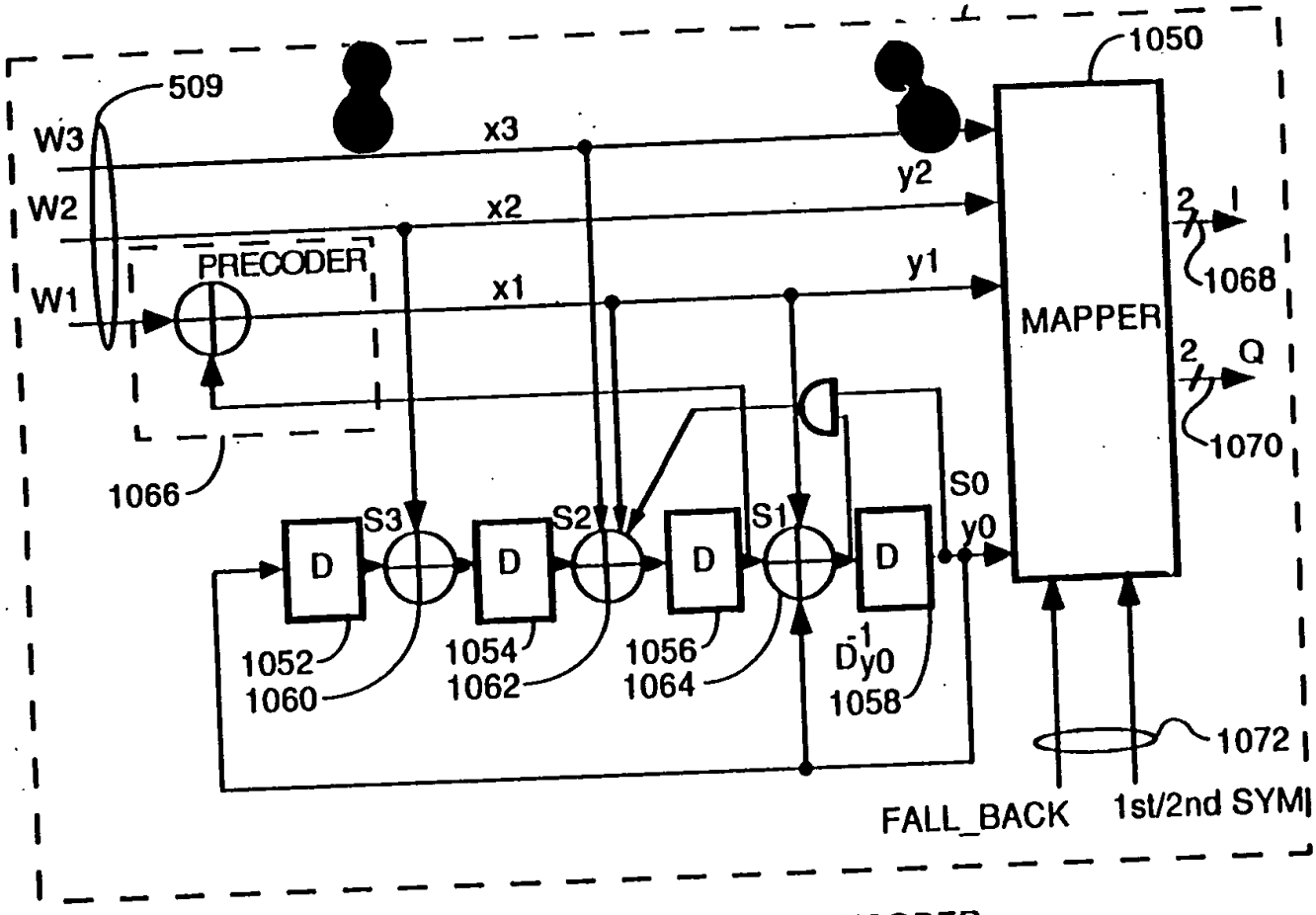

PAGE 1
MEMORY 300
144
ADDR
LOCATIONS
SYMBOL 3
SYMBOL 2
SYMBOL 1
TB1
TB2
TB3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS
3 BITS
3 BITS

FIG. 20

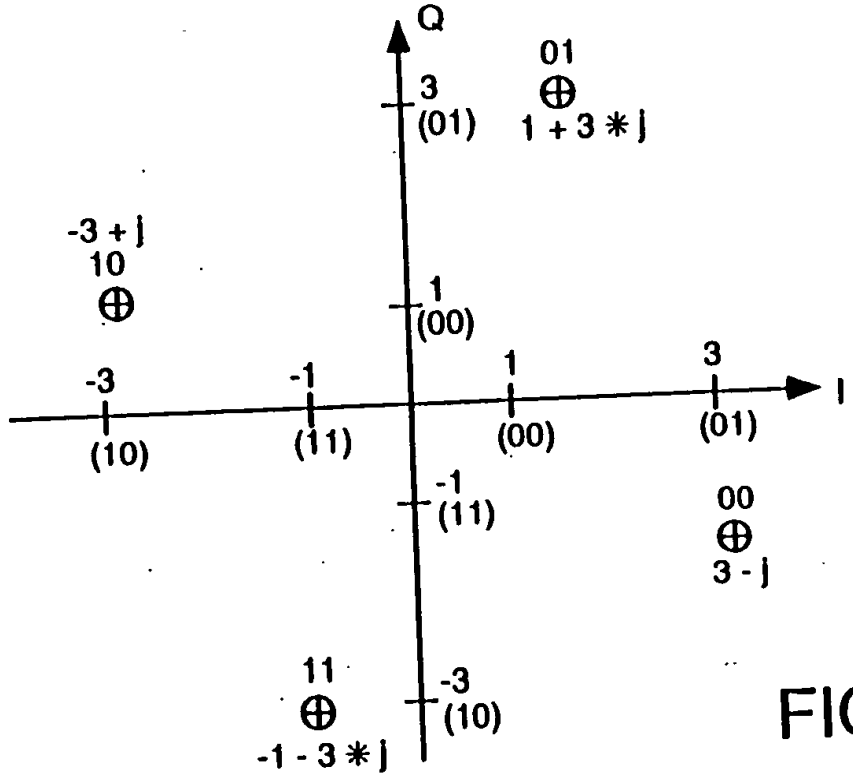


PREFERRED TRELLIS ENCODER

FIG. 42

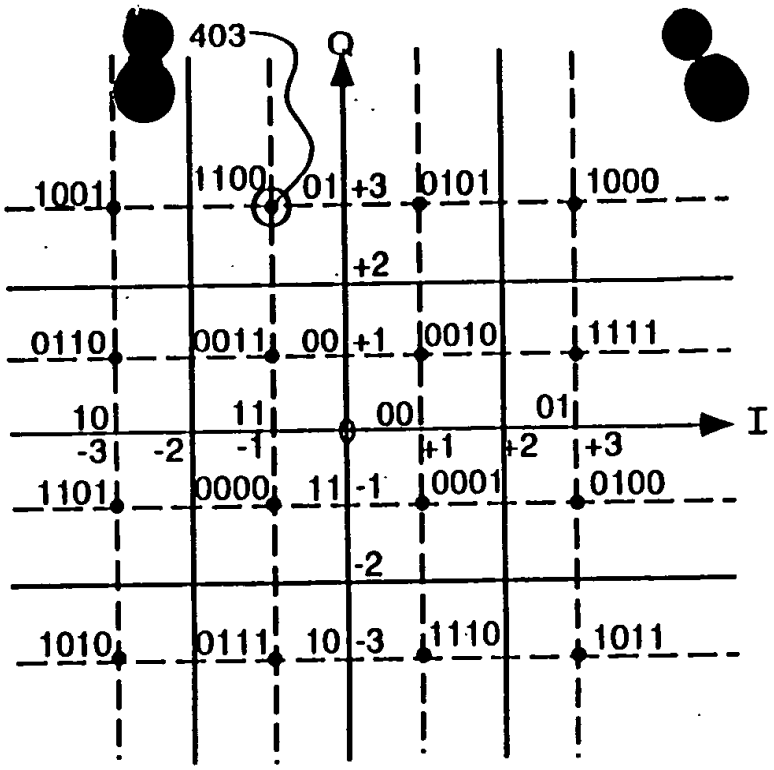
17

MAPPING FOR FALL-BACK MODE - LSB'S



21

FIG. 43



18

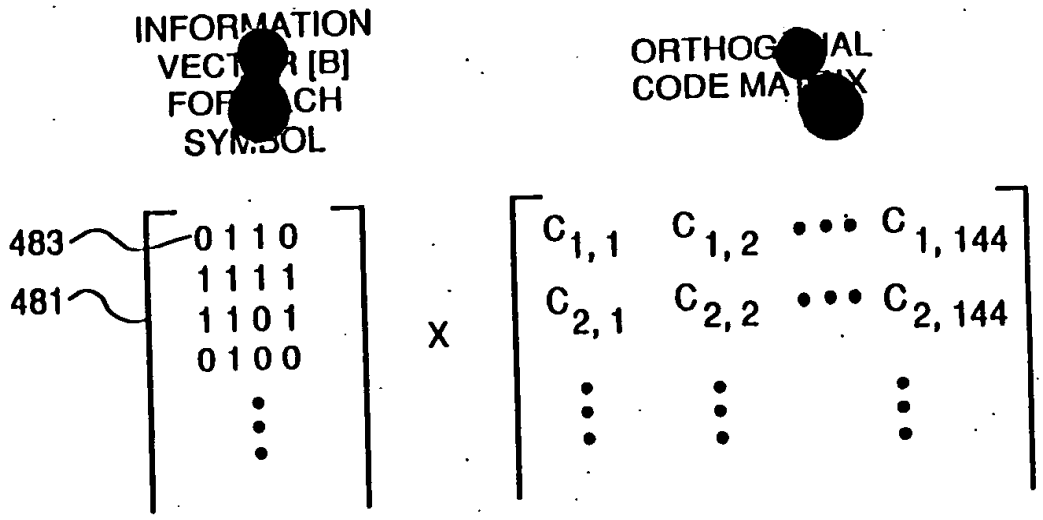
FIG. 21

CODE	INPHASE	QUADRATURE	
0000	111	111	= -1 - j
0001	001	111	= 1 - j
0010	001	001	= 1+ j
0011	111	001	= -1+ j
0100	011	111	= 3 - j
0101	001	011	= 1+ 3* j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3* j
1000	011	011	=+3 + 3* j
1001	101	011	= -3 + 3* j
1010	101	101	= -3 - 3* j
1011	011	101	= 3 - 3* j
1100	111	011	= -1+ 3* j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3* j
1111	011	001	= 3 + j

403

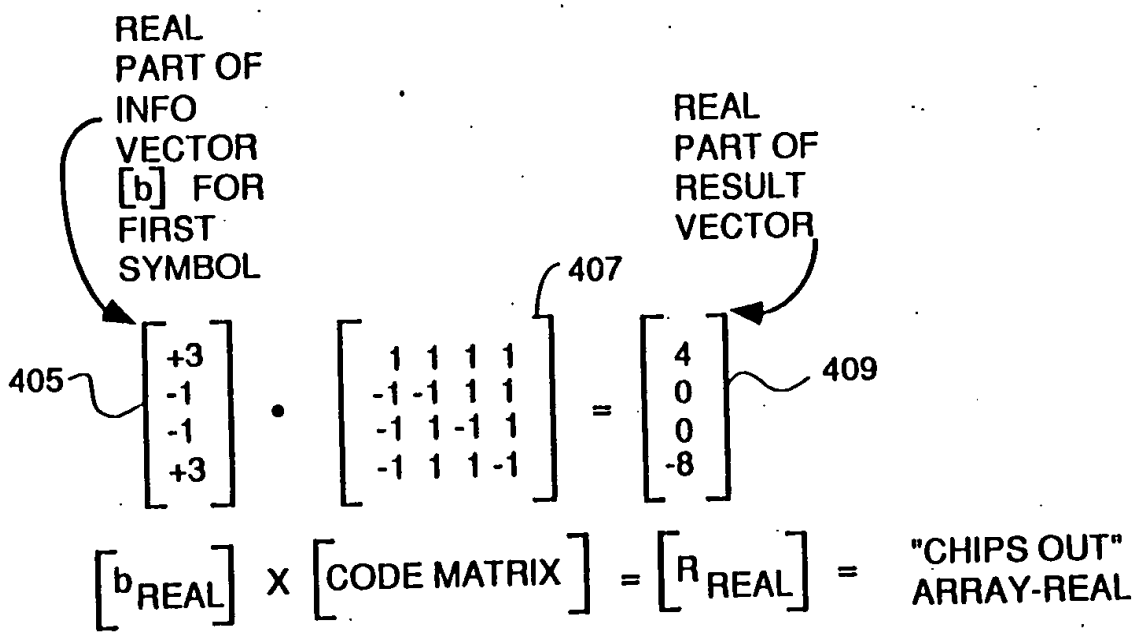
19

FIG. 22



20A

FIG. ~~23~~A



20B

FIG. ~~23~~B

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. ~~44~~ 22

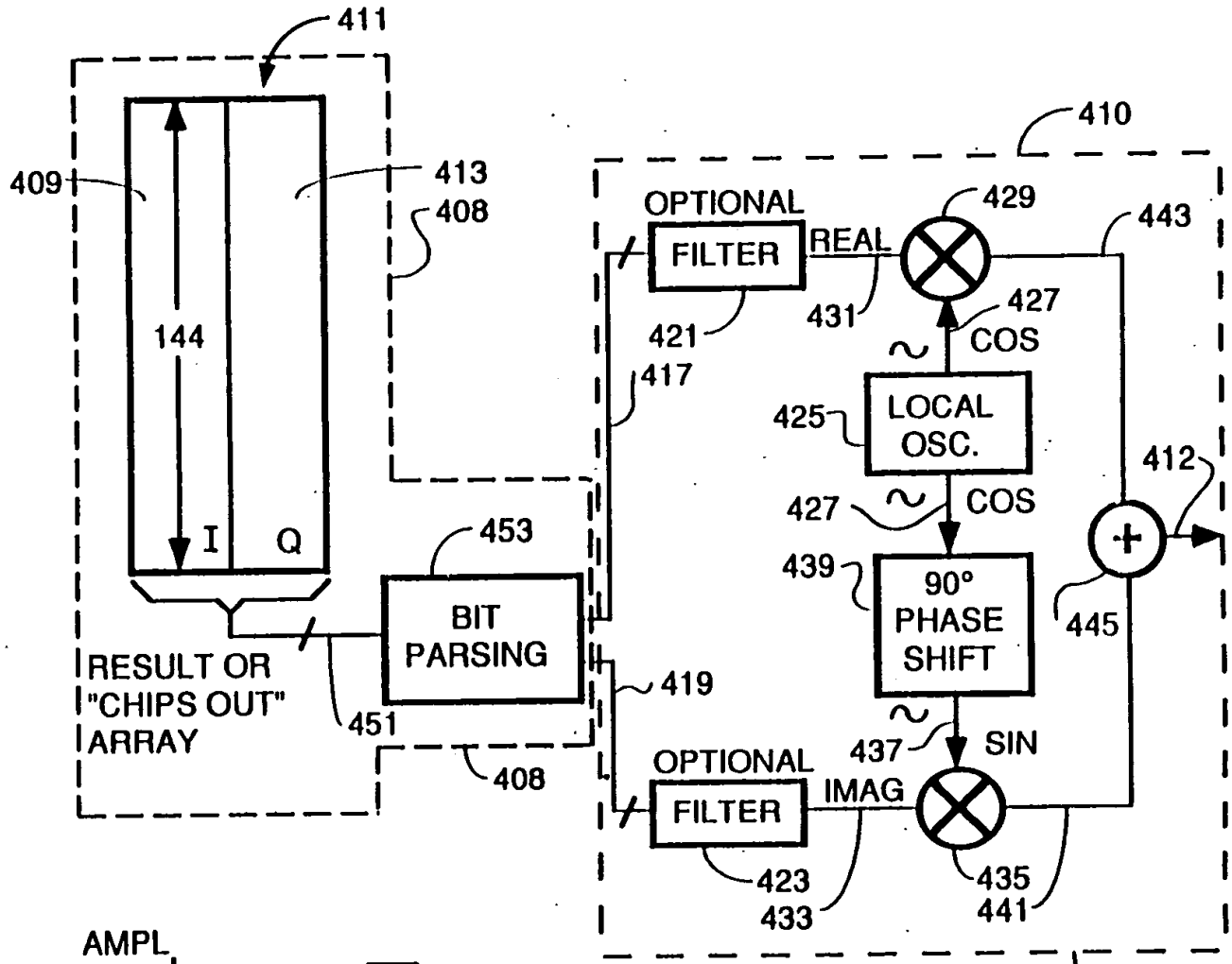

411
409
413
408
144
I
Q
453
BIT PARSING
RESULT OR "CHIPS OUT" ARRAY
451
408
410
OPTIONAL
FILTER
REAL
421
429
431
443
427
COS
417
425
LOCAL OSC.
427
COS
412
439
90° PHASE SHIFT
445
419
437
SIN
OPTIONAL
FILTER
IMAG
423
433
435
441
410

FIG. 24

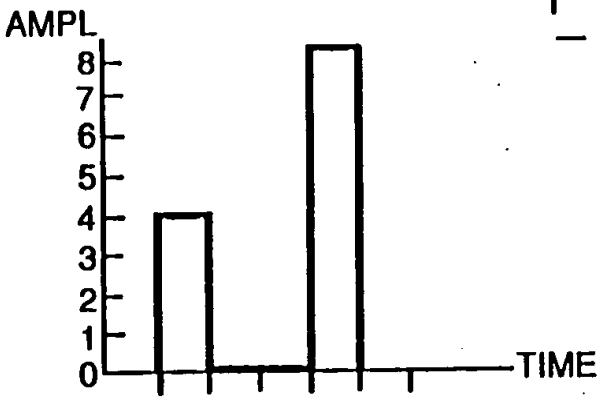
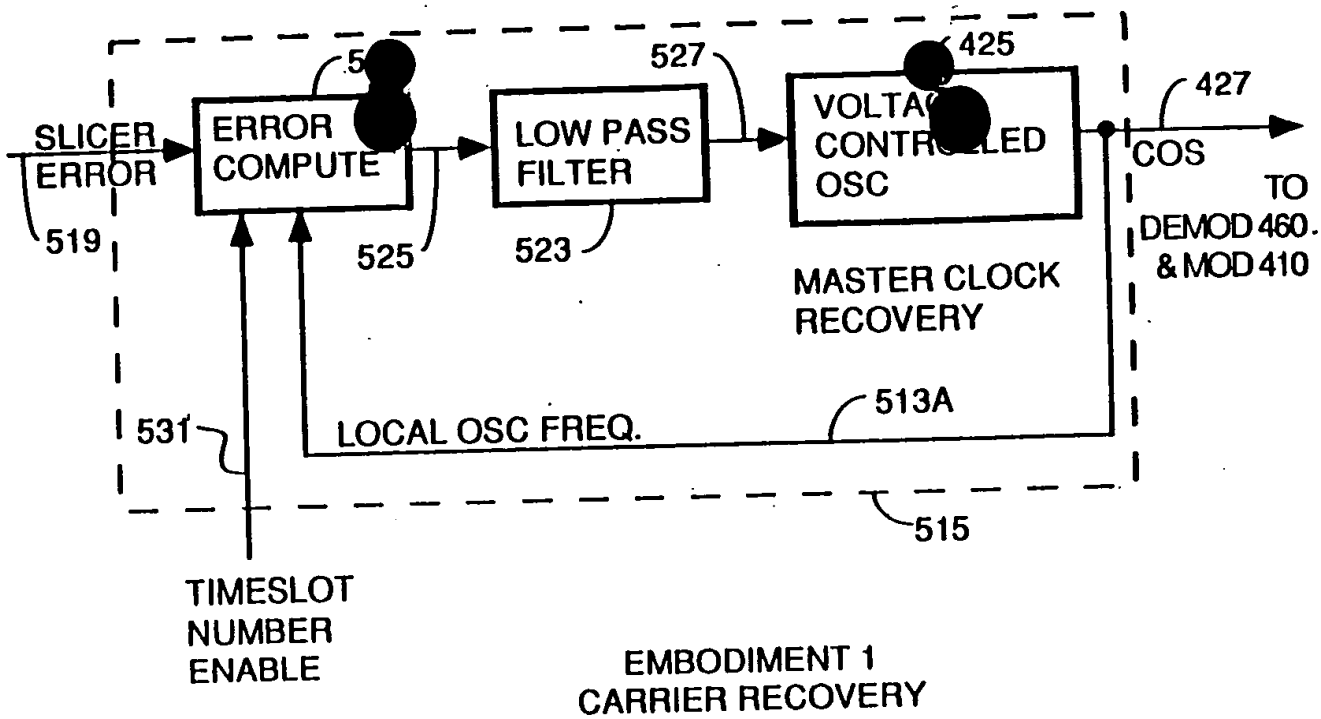

AMPL
8
7
6
5
4
3
2
1
0
TIME

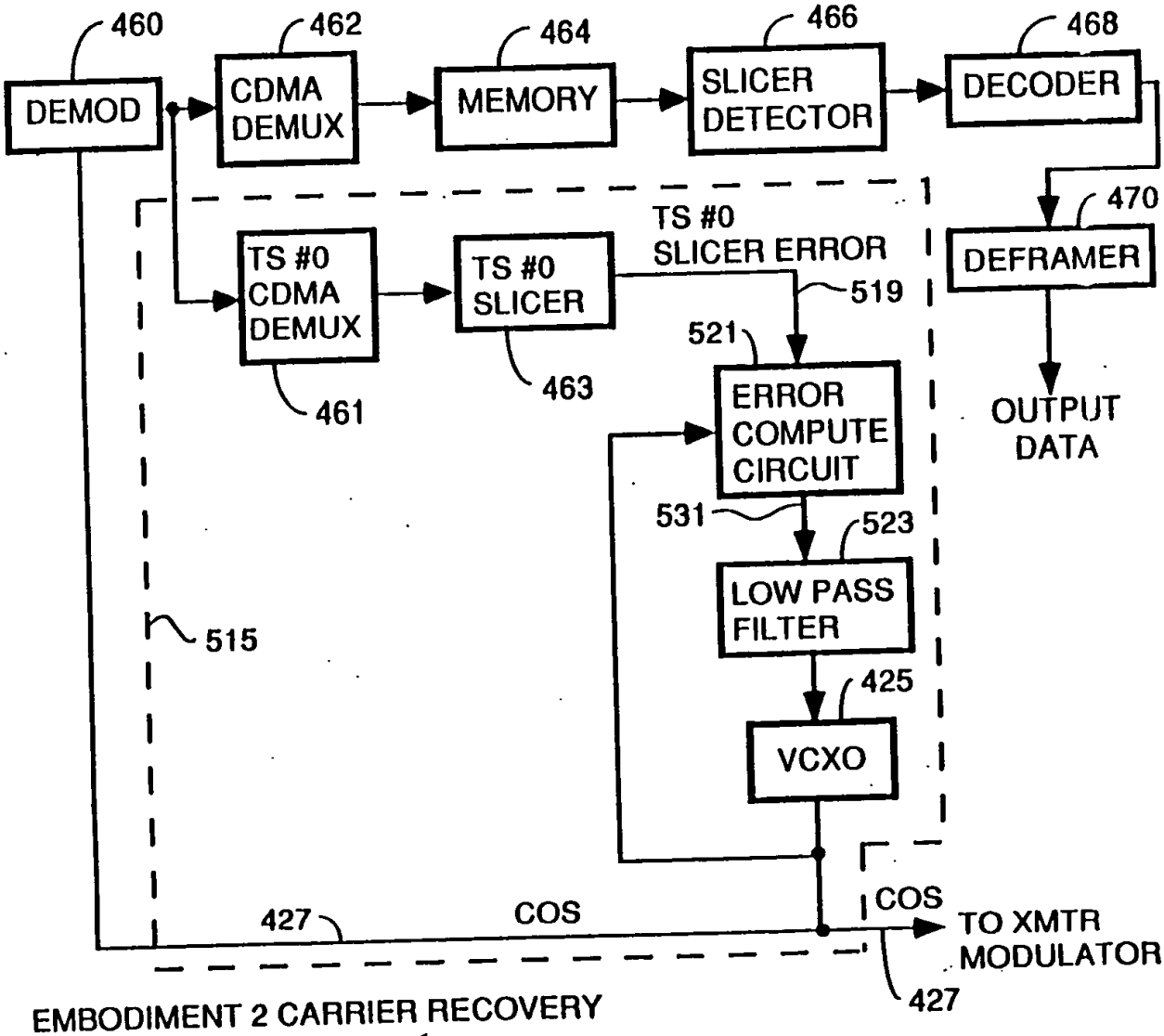
FIG. 25



EMBODIMENT 1
CARRIER RECOVERY

FIG. 35

25



EMBODIMENT 2 CARRIER RECOVERY

FIG. 36

26

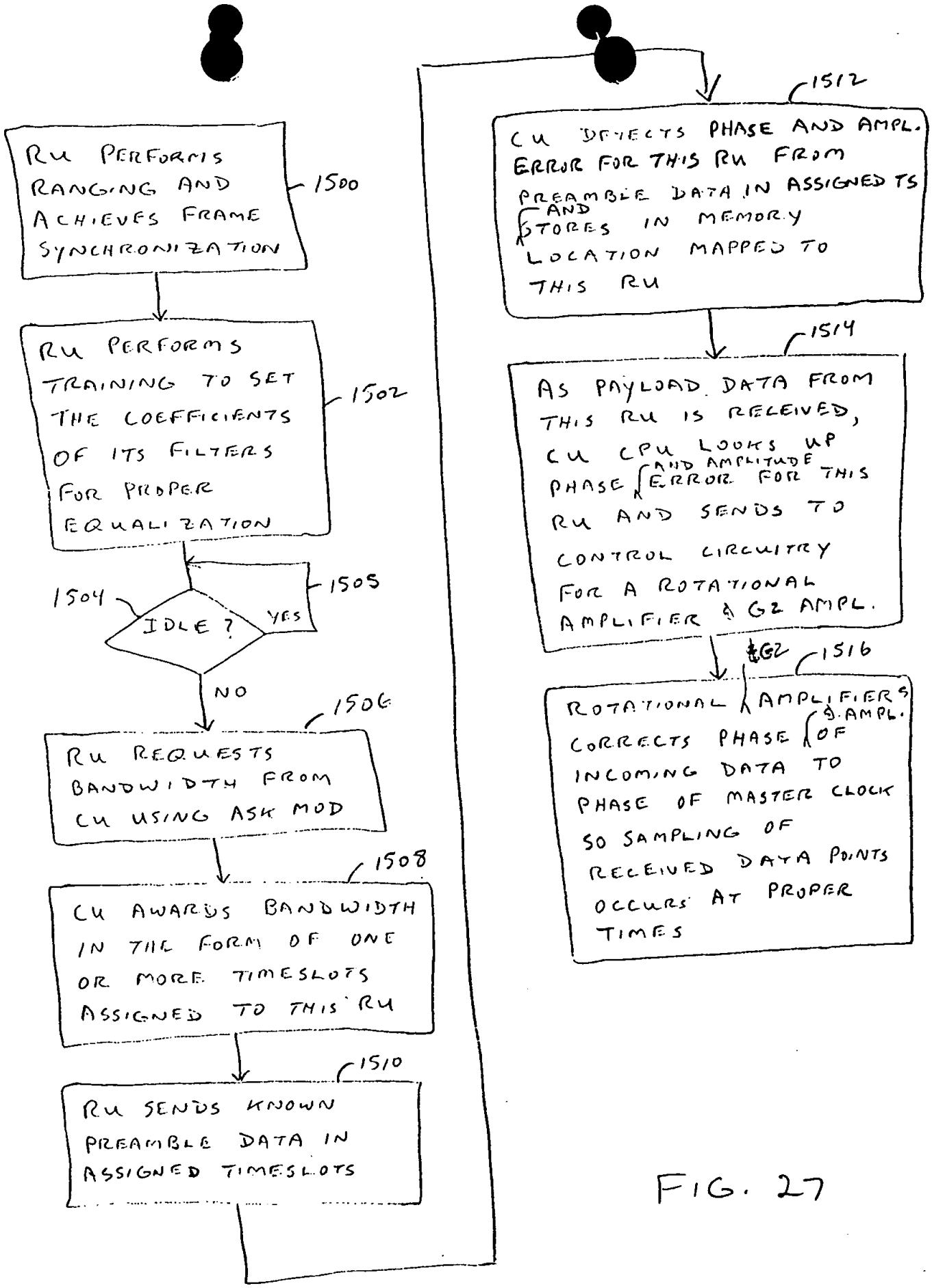
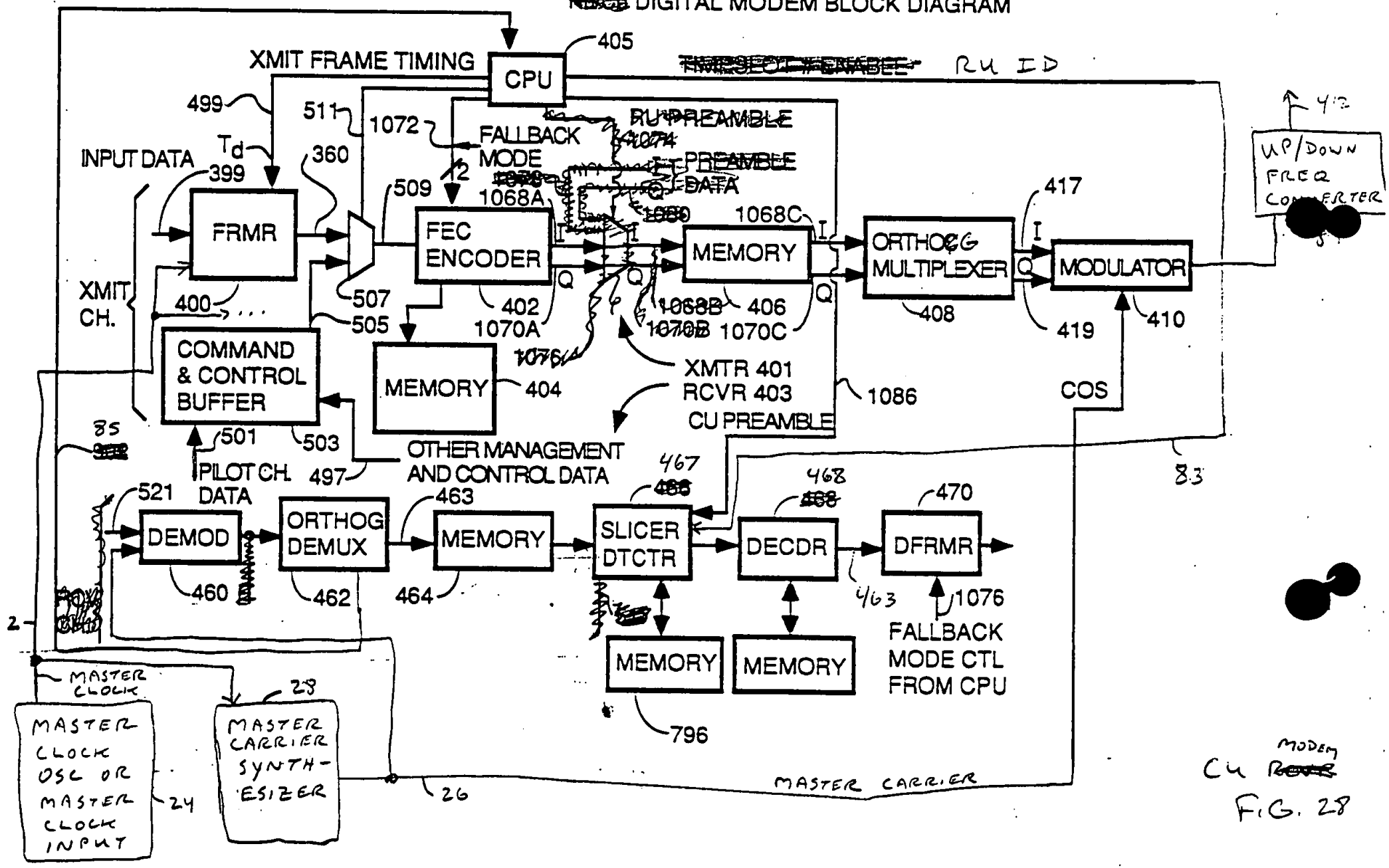

RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1500
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1502
1504
IDLE ?
YES
1505
NO
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1506
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1508
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1510
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED TS AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1512
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1514
G2
ROTATIONAL AMPLIFIERS & AMPL. CORRECTS PHASE OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES
1516

FIG. 27

CU

DIGITAL MODEM BLOCK DIAGRAM



CU MODEM

FIG. 28

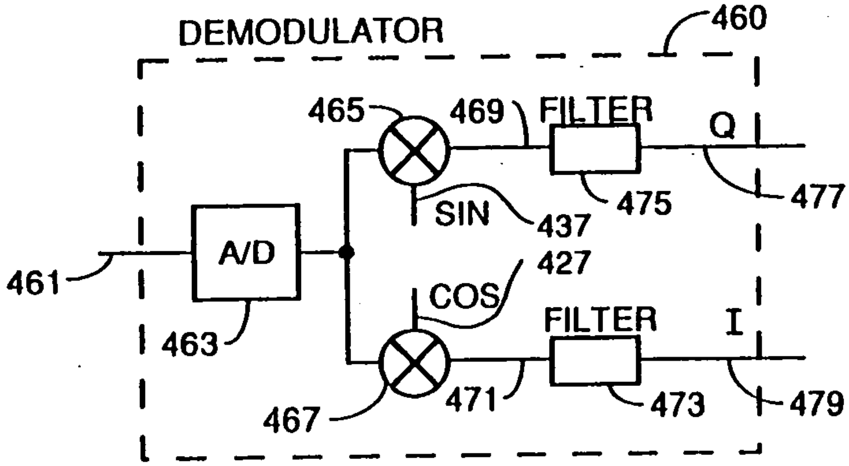

DEMODULATOR
460
465
469
FILTER
Q
477
475
SIN
437
461
A/D
427
COS
463
FILTER
I
467
471
473
479

FIG. ~~26~~ 29

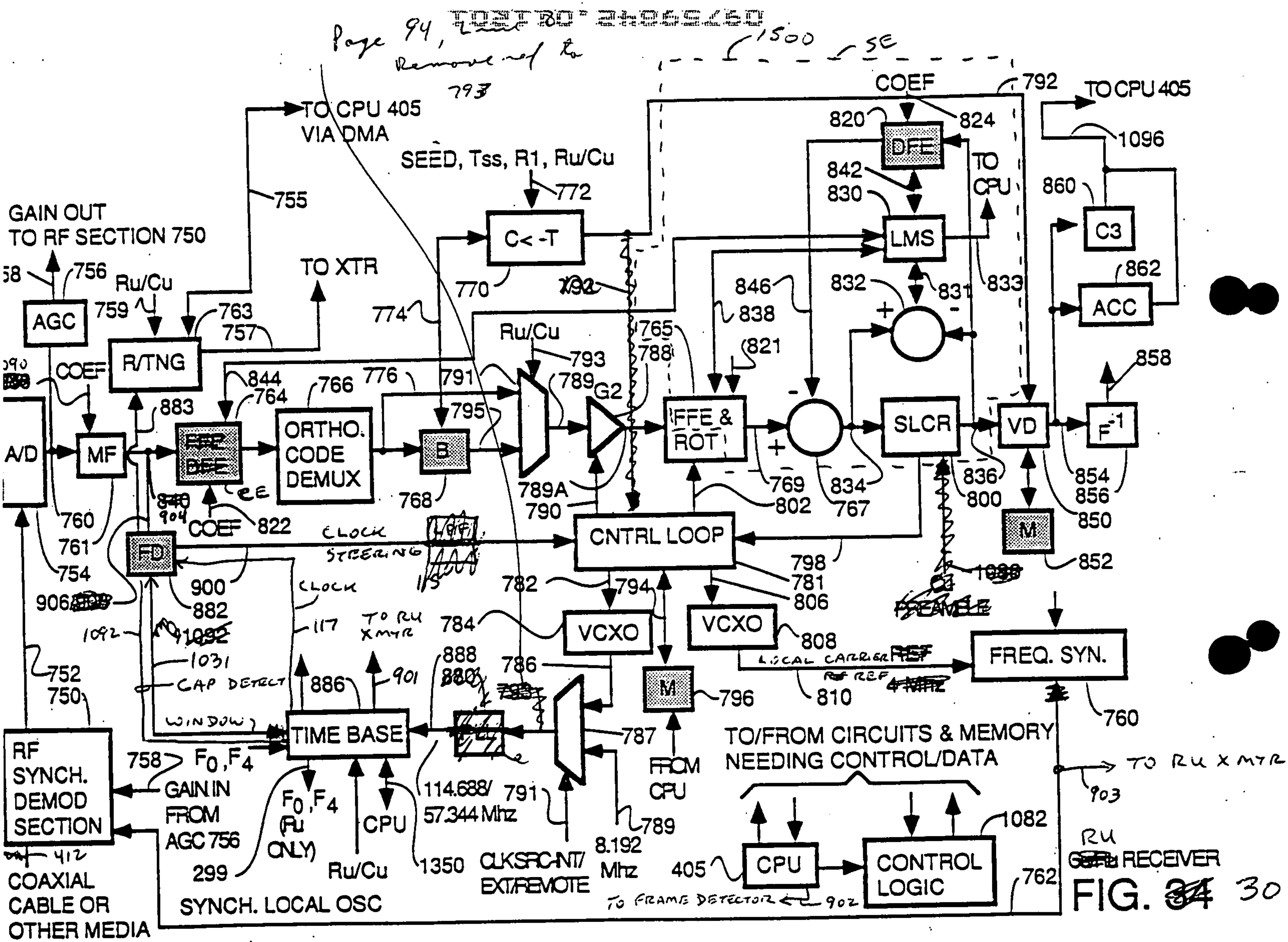

GAIN OUT TO RF SECTION 750
AGC
R/TNG
TO CPU 405 VIA DMA
TO XTR
SEED, Tss, R1, Ru/Cu
C< -T
A/D
MF
ORTHO. CODE DEMUX
B
Ru/Cu
G2
FFE & ROT
SLCR
VD
LMS
DFE
COEF
TO CPU
TO CPU 405
C3
ACC
CNTRL LOOP
VCXO
M
FD
TIME BASE
FREQ. SYN.
CPU
CONTROL LOGIC
TO/FROM CIRCUITS & MEMORY NEEDING CONTROL/DATA
RF SYNCH. DEMOD SECTION
COAXIAL CABLE OR OTHER MEDIA
SYNCH. LOCAL OSC
GAIN IN FROM AGC 756
114.688/ 57.344 Mhz
8.192 Mhz
CLKSRC-INT/ EXT/REMOTE
FROM CPU
RU RECEIVER

FIG. 30

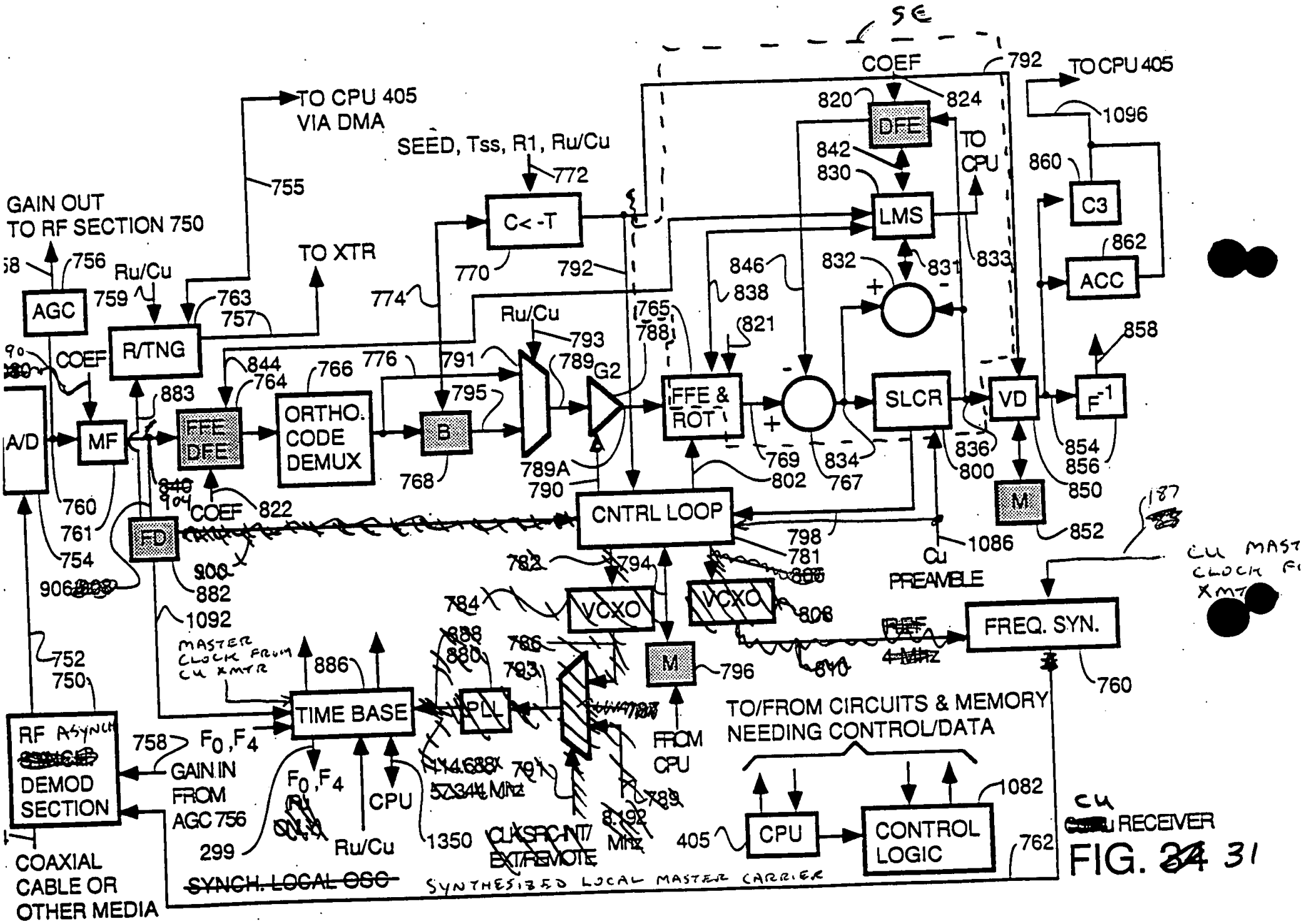

5E
TO CPU 405
VIA DMA
SEED, Tss, R1, Ru/Cu
772
755
GAIN OUT
TO RF SECTION 750
TO XTR
C<-T
770
792
COEF
792
TO CPU 405
820
824
DFE
1096
842
830
TO
CPU
LMS
860
C3
862
ACC
846
838
832
831
833
774
Ru/Cu
765
788
821
858
AGC
756
Ru/Cu
759
763
757
R/TNG
COEF
844
764
766
776
791
793
789
G2
795
883
FFE
DFE
ORTHO.
CODE
DEMUX
B
FFE &
ROT
SLCR
VD
F-1
A/D
MF
768
789A
790
769
834
802
767
836
800
854
856
850
760
761
754
COEF
822
CNTRL LOOP
798
781
1086
Cu
PREAMBLE
M
852
FD
882
1092
782
794
784
VCXO
VCXO
808
FREQ. SYN.
752
750
MASTER
CLOCK FROM
CU XMTR
886
888
880
786
793
M
796
TIME BASE
PLL
FROM
CPU
TO/FROM CIRCUITS & MEMORY
NEEDING CONTROL/DATA
RF ASYNCH
DEMOD
SECTION
758
F0, F4
GAIN IN
FROM
AGC 756
F0, F4
CPU
791
789
1082
405
CPU
CONTROL
LOGIC
762
299
Ru/Cu
1350
CLKSRC-INT/
EXT/REMOTE
8.192
MHz
SYNTHESIZED LOCAL MASTER CARRIER
COAXIAL
CABLE OR
OTHER MEDIA
CU
RECEIVER

FIG. 24 31

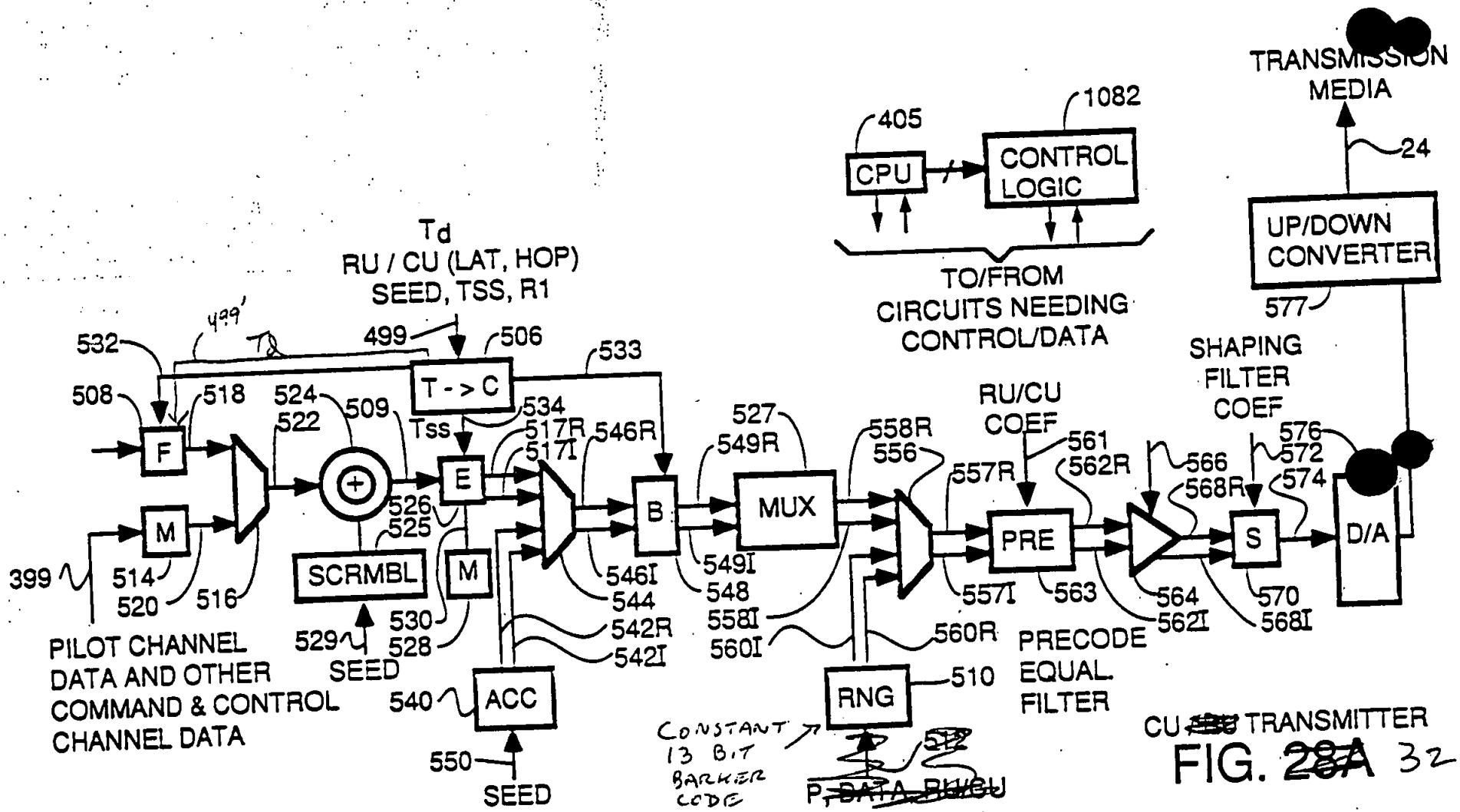

TRANSMISSION MEDIA
24
UP/DOWN CONVERTER
577
1082
405
CPU
CONTROL LOGIC
TO/FROM CIRCUITS NEEDING CONTROL/DATA
Td
RU / CU (LAT, HOP) SEED, TSS, R1
499'
Td
499
506
533
532
508
518
524
522
509
T -> C
534
Tss
517R
517I
546R
527
549R
558R
556
RU/CU COEF
561
562R
557R
SHAPING FILTER COEF
576
572
566
568R
574
F
E
B
MUX
PRE
S
D/A
M
526
525
546I
544
549I
548
557I
563
564
562I
570
568I
399
514
520
516
SCRMBL
M
530
528
542R
542I
558I
560I
560R
529
SEED
PILOT CHANNEL DATA AND OTHER COMMAND & CONTROL CHANNEL DATA
PRECODE EQUAL FILTER
540
ACC
550
SEED
RNG
510
CONSTANT 13 BIT BARKER CODE
P, DATA RU/CU
CU TRANSMITTER

FIG. 28A 32

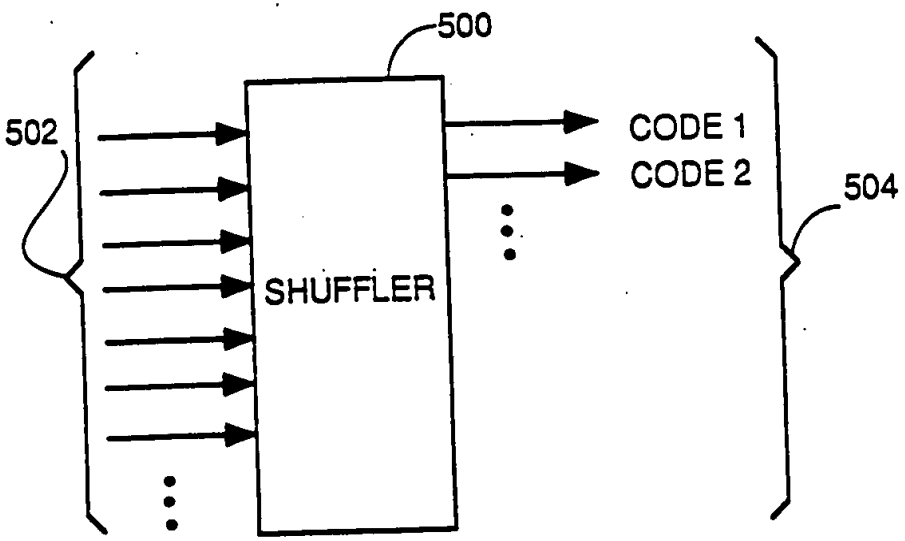


FIG. 27 38

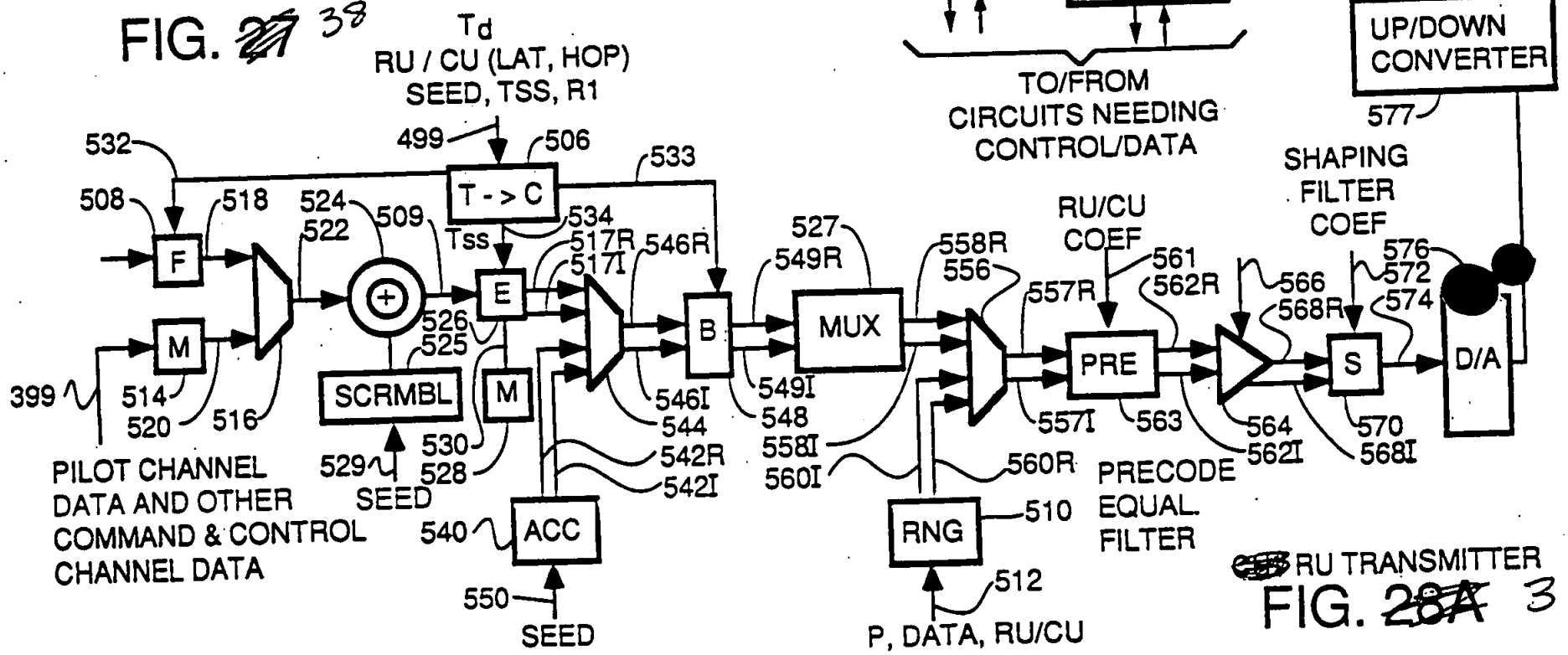
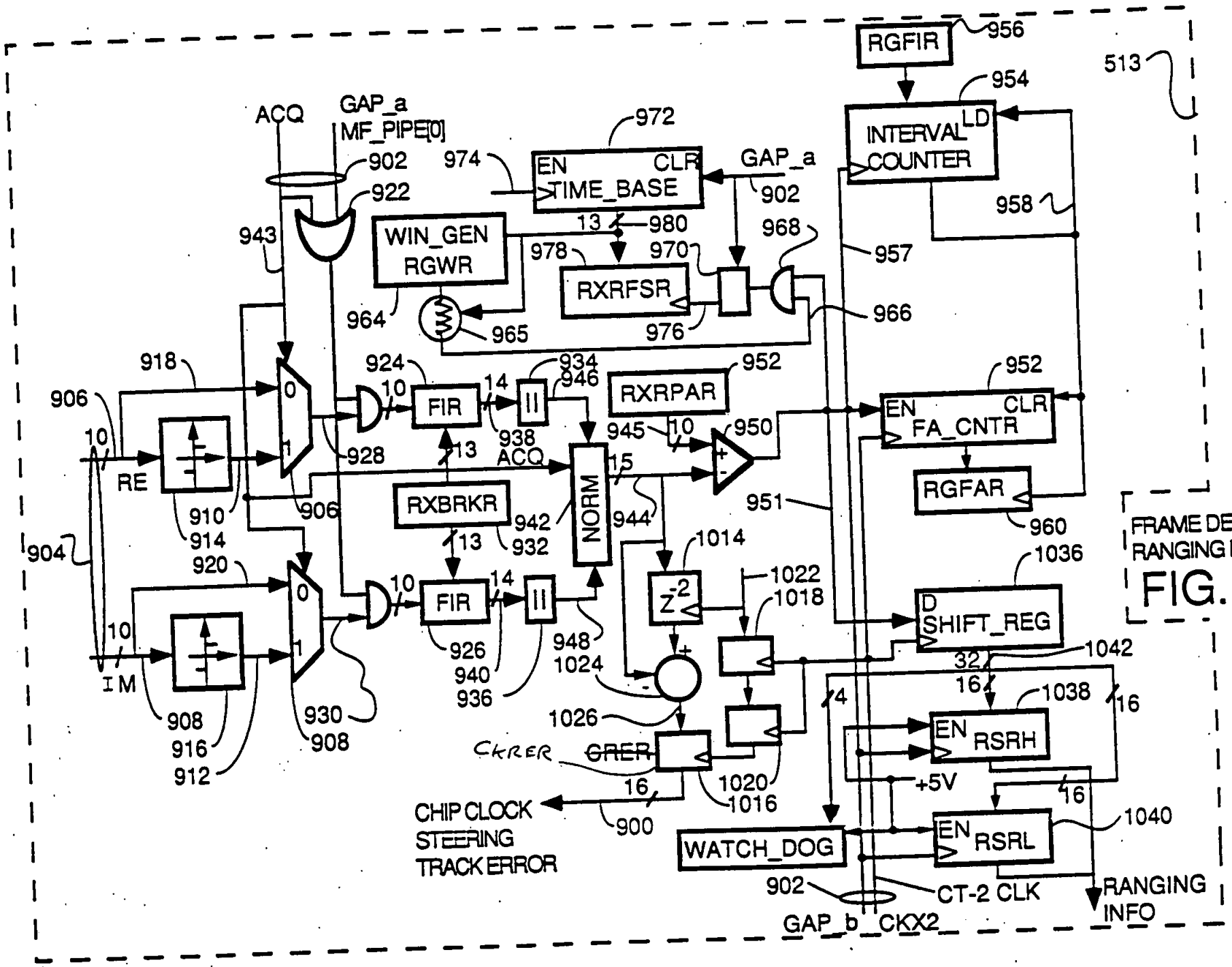


FIG. 28A 3


RGFIR
956
513
954
INTERVAL COUNTER
LD
958
957
ACQ
GAP_a
MF_PIPE[0]
902
922
943
974
EN
CLR
TIME_BASE
972
GAP_a
902
WIN_GEN
RGWR
13
980
968
978
970
RXRFSR
964
965
976
966
906
918
924
10
FIR
14
934
946
RXRPAR
952
952
EN
CLR
FA_CNTR
945
10
950
928
13
ACQ
15
RE
10
910
914
906
RXBRKR
942
932
NORM
944
951
RGFAR
960
904
920
1014
1036
FRAME DETECTOR/
RANGING DETECTOR
FIG. 3B
10
FIR
14
1022
1018
D
SHIFT_REG
926
940
936
948
1024
1042
32
16
1038
16
IM
908
916
912
930
908
1026
EN
RSRH
4
CKRER
GRER
+5V
16
1020
1016
16
CHIP CLOCK
STEERING
TRACK ERROR
900
WATCH_DOG
EN
RSRL
1040
902
CT-2 CLK
RANGING
INFO
GAP_b
CKX2

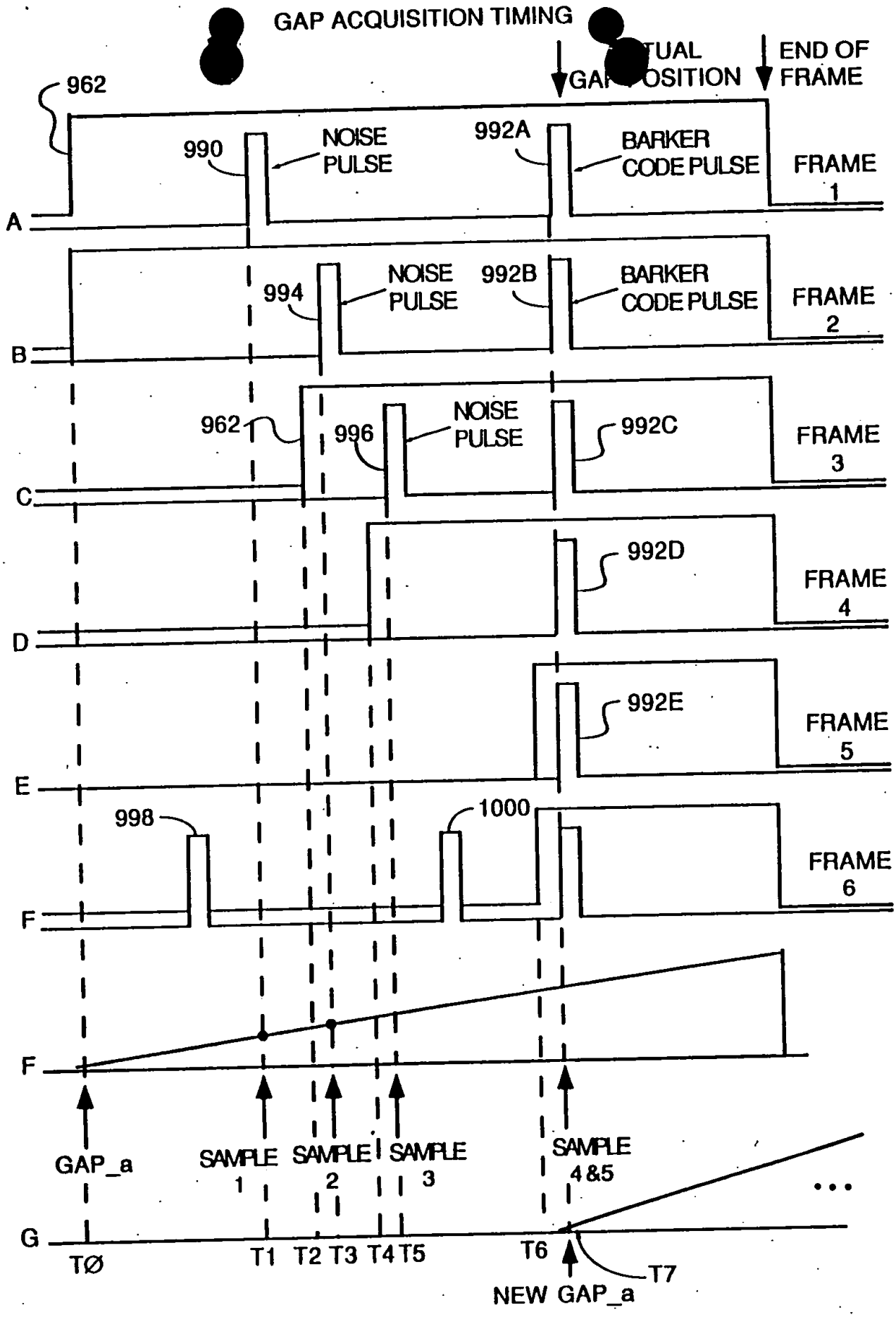
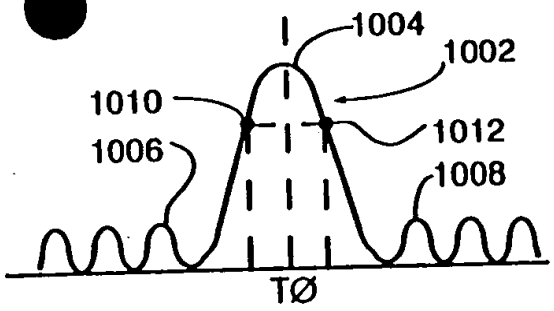
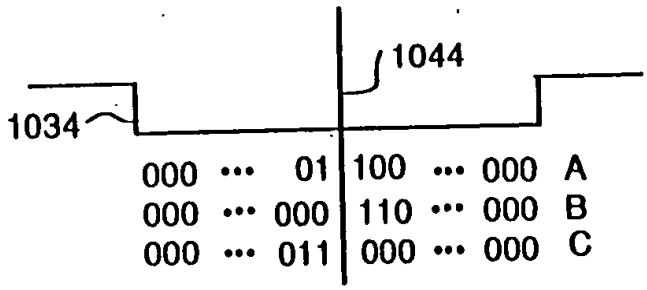

GAP ACQUISITION TIMING
ACTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4&5
G
TØ
T1 T2 T3 T4 T5
T6
T7
NEW GAP_a

FIG. 39 35



36

FIG. ~~40~~



37

FIG. ~~41~~

FINE TUNING TO CENTER BARRIER CODE

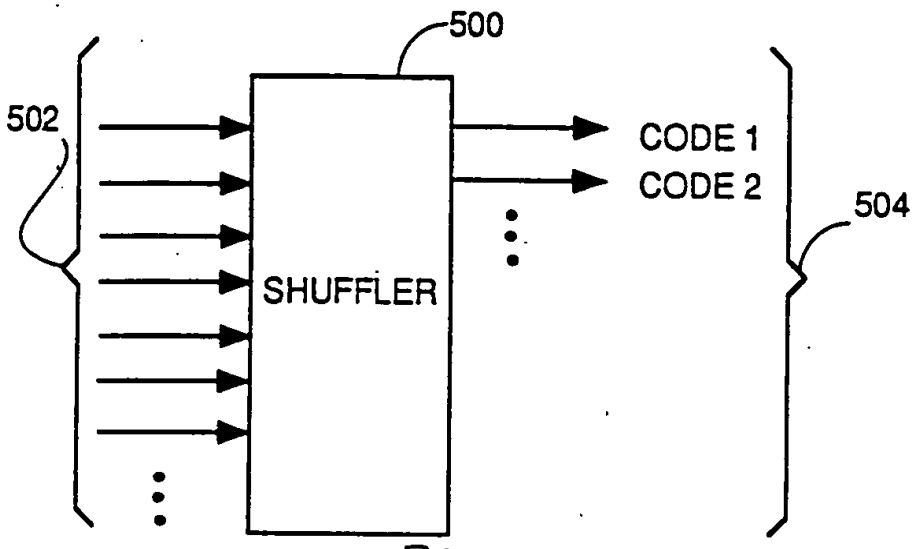


FIG. 27

38

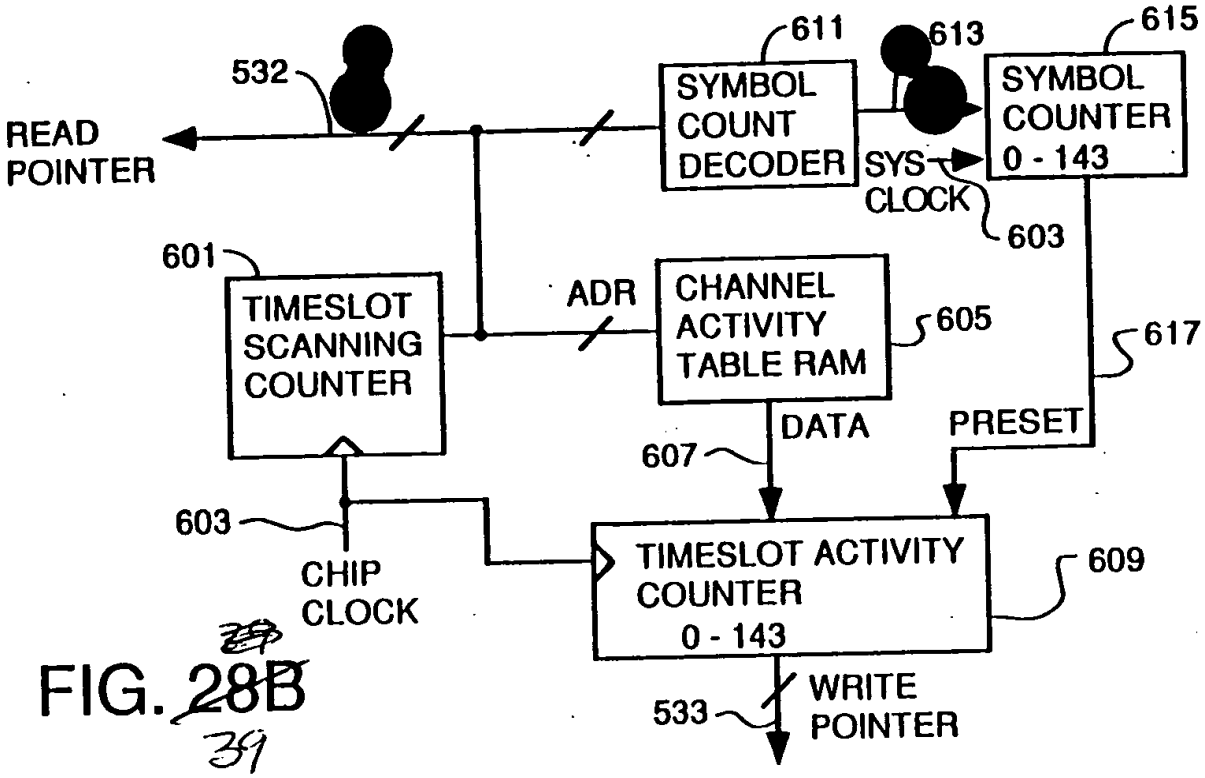


FIG. 28B

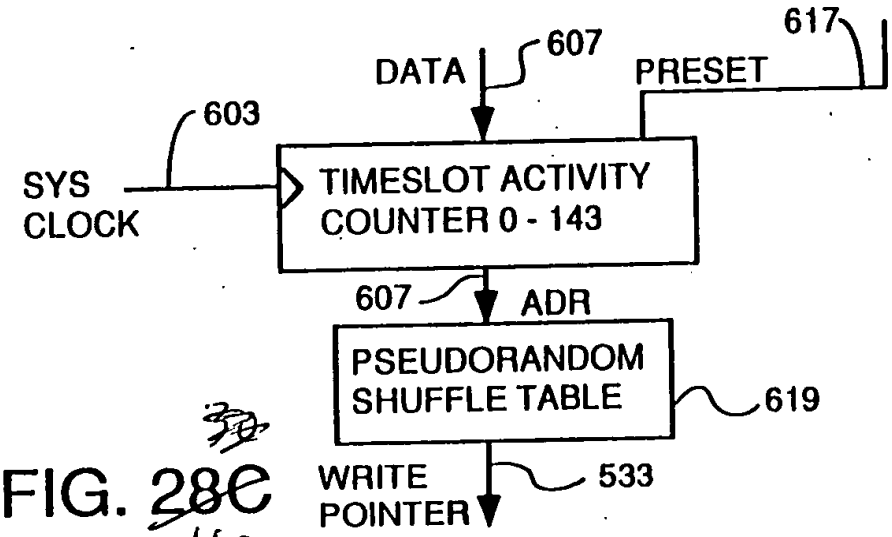


FIG. 28C

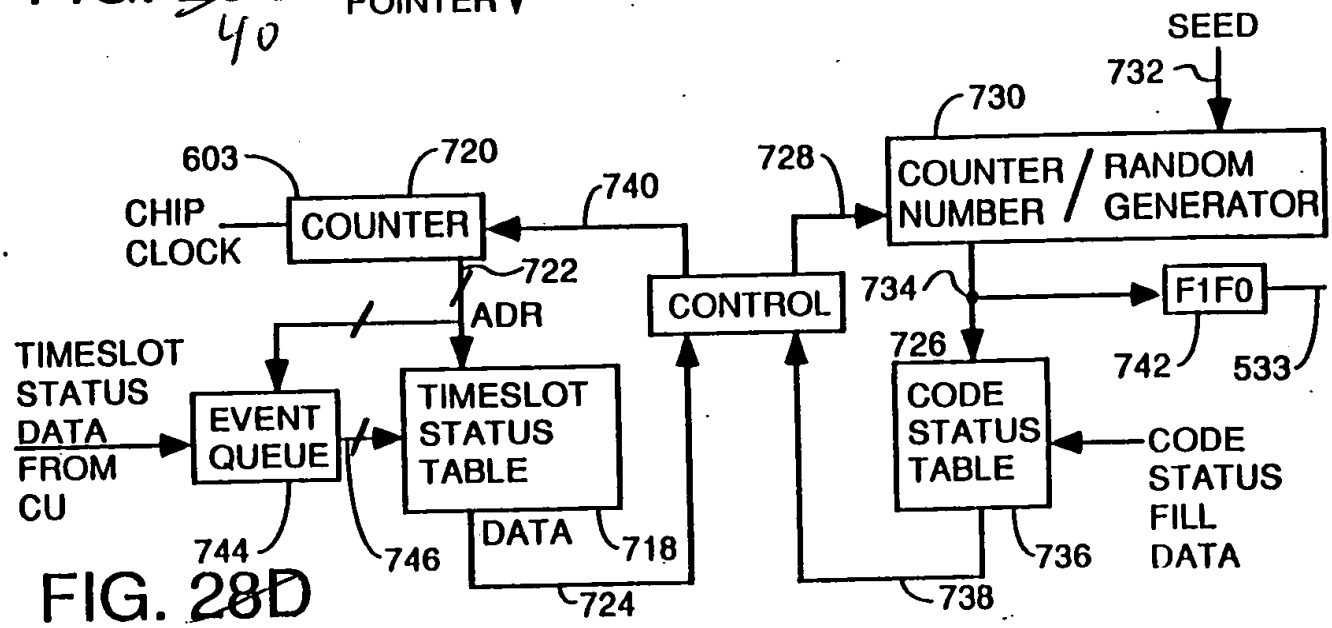
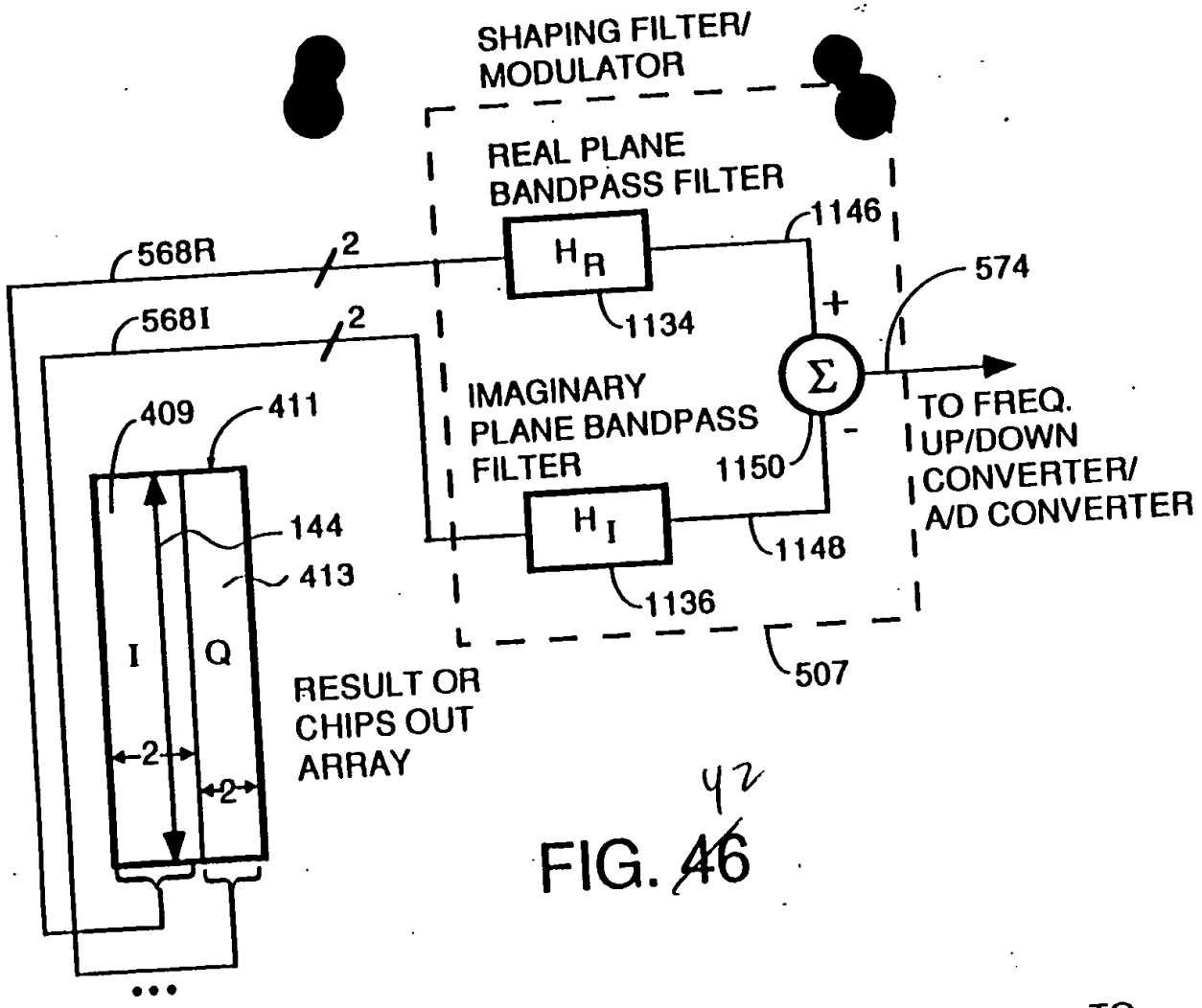
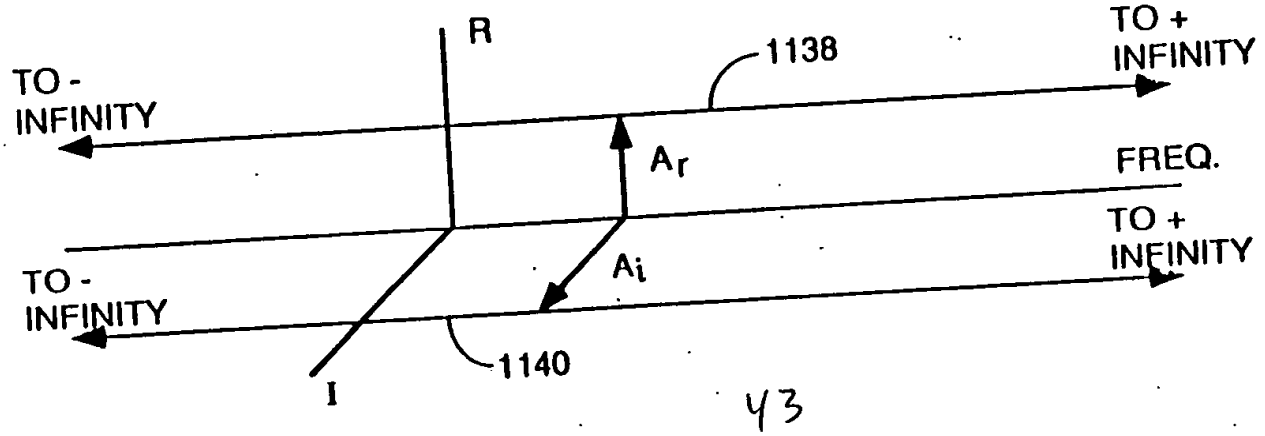


FIG. 28D



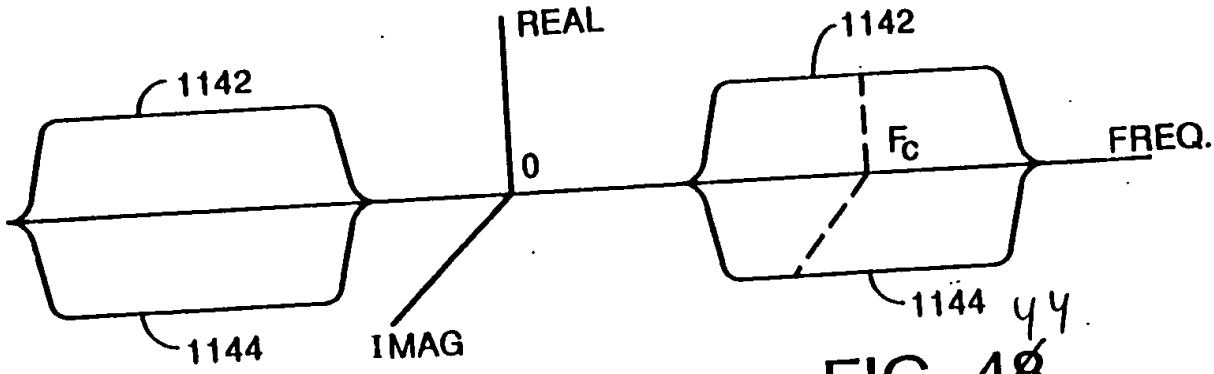
42

FIG. 46



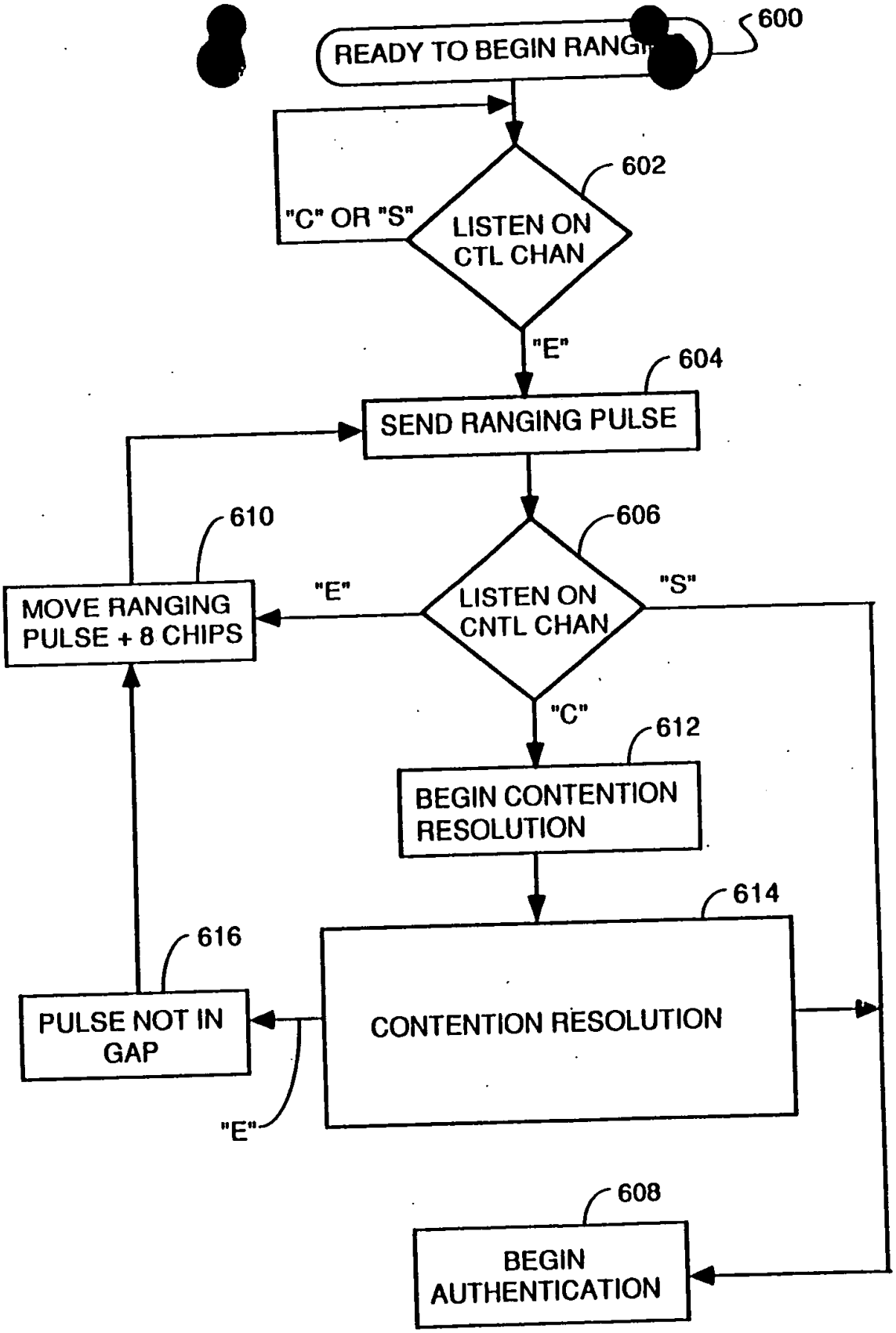
43

FIG. 47



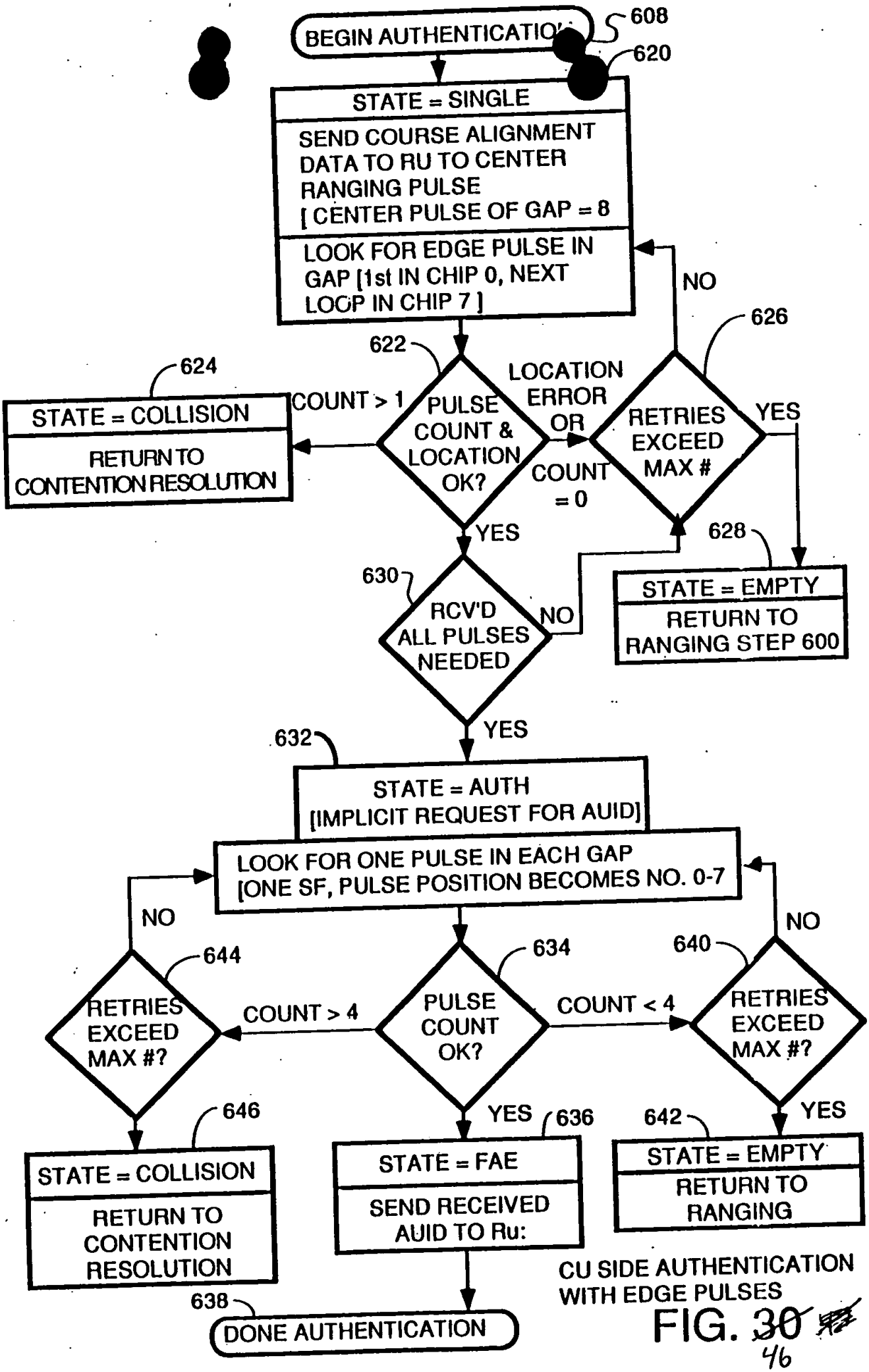
44

FIG. 48



RU RANGING

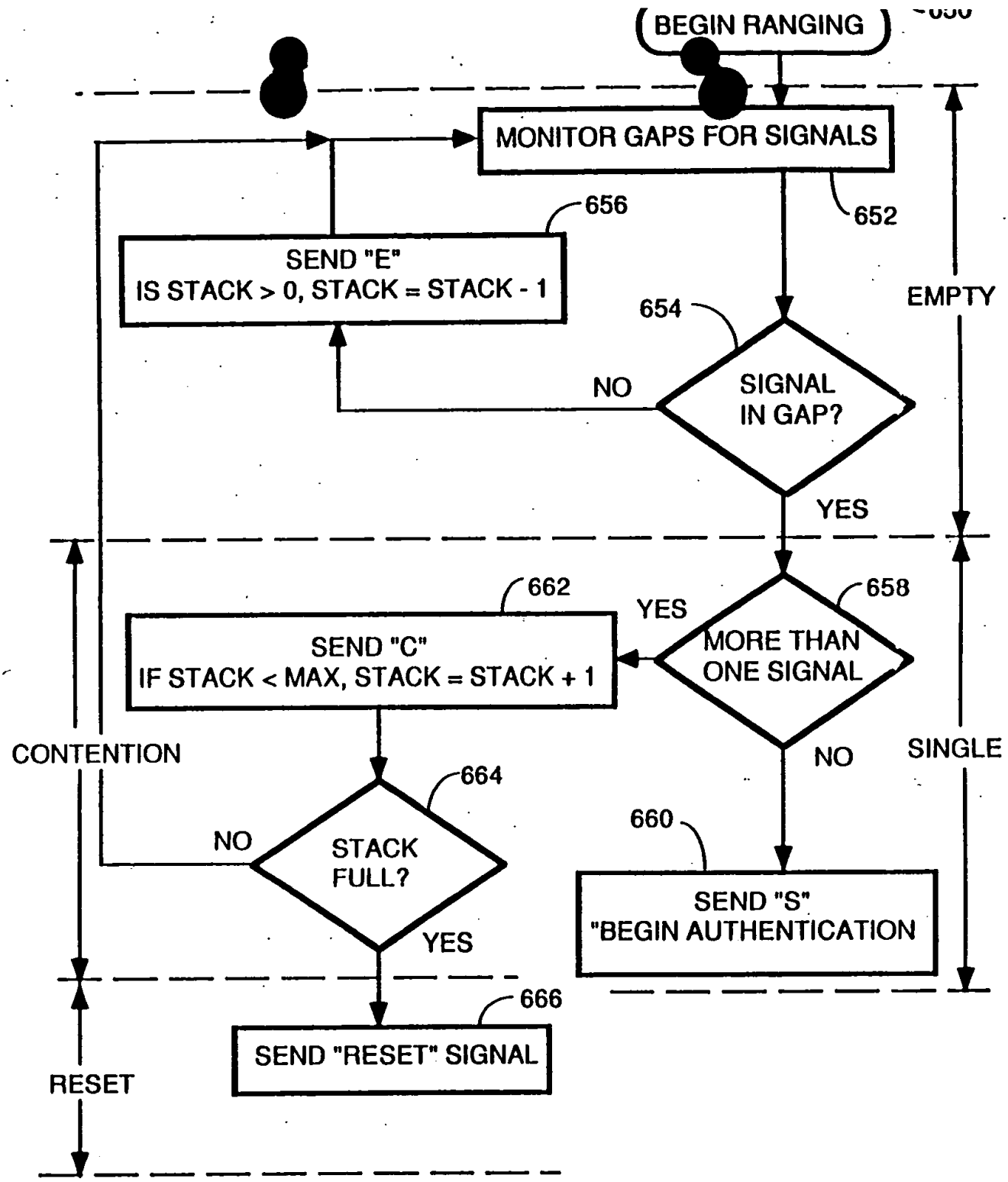
FIG. 29



CU SIDE AUTHENTICATION WITH EDGE PULSES

FIG. 30

46

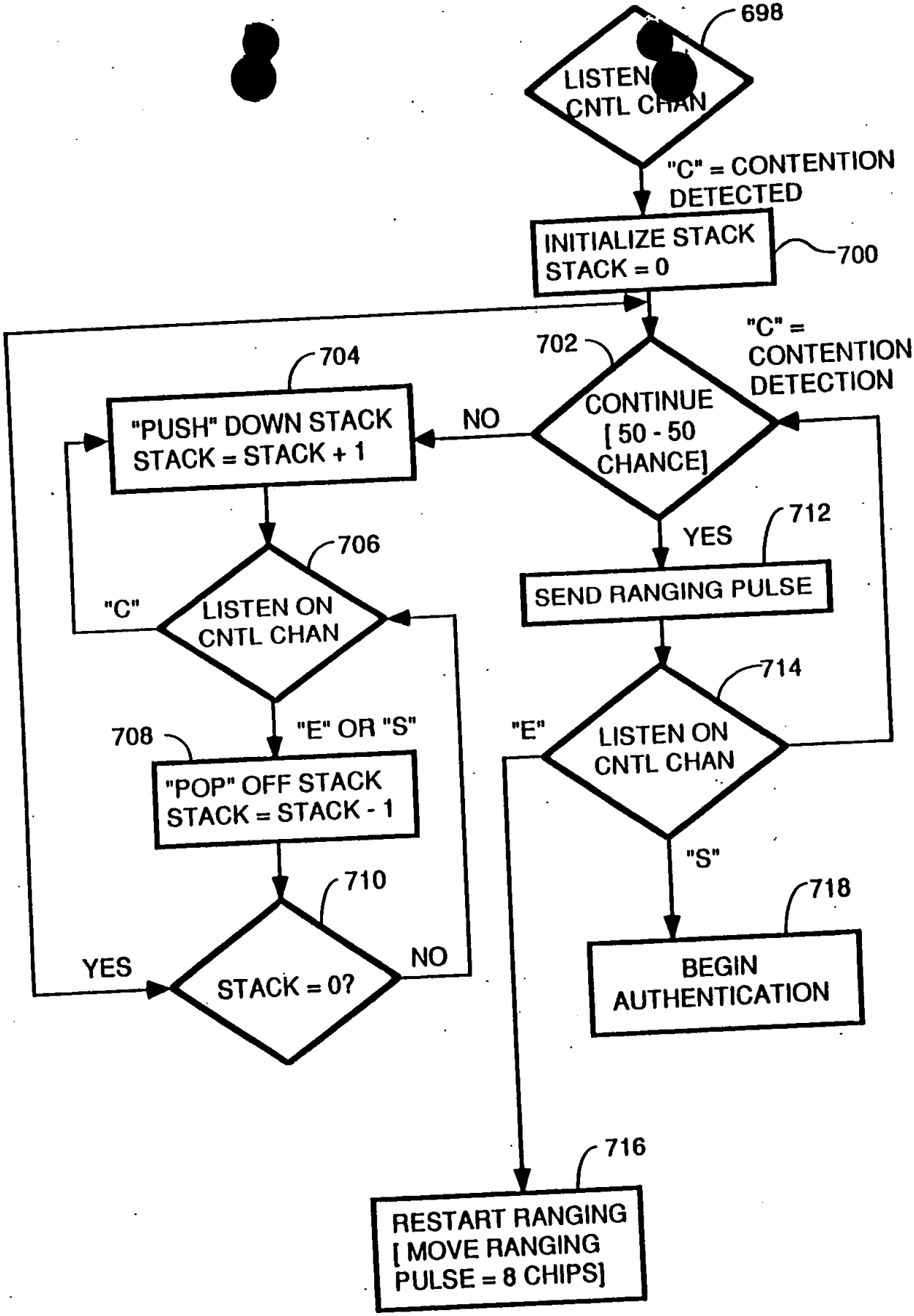


CU RANGING & CONTENTION RESOLUTION

~~RANGING AND CONTENTION RESOLUTION~~
~~CU SIDE~~

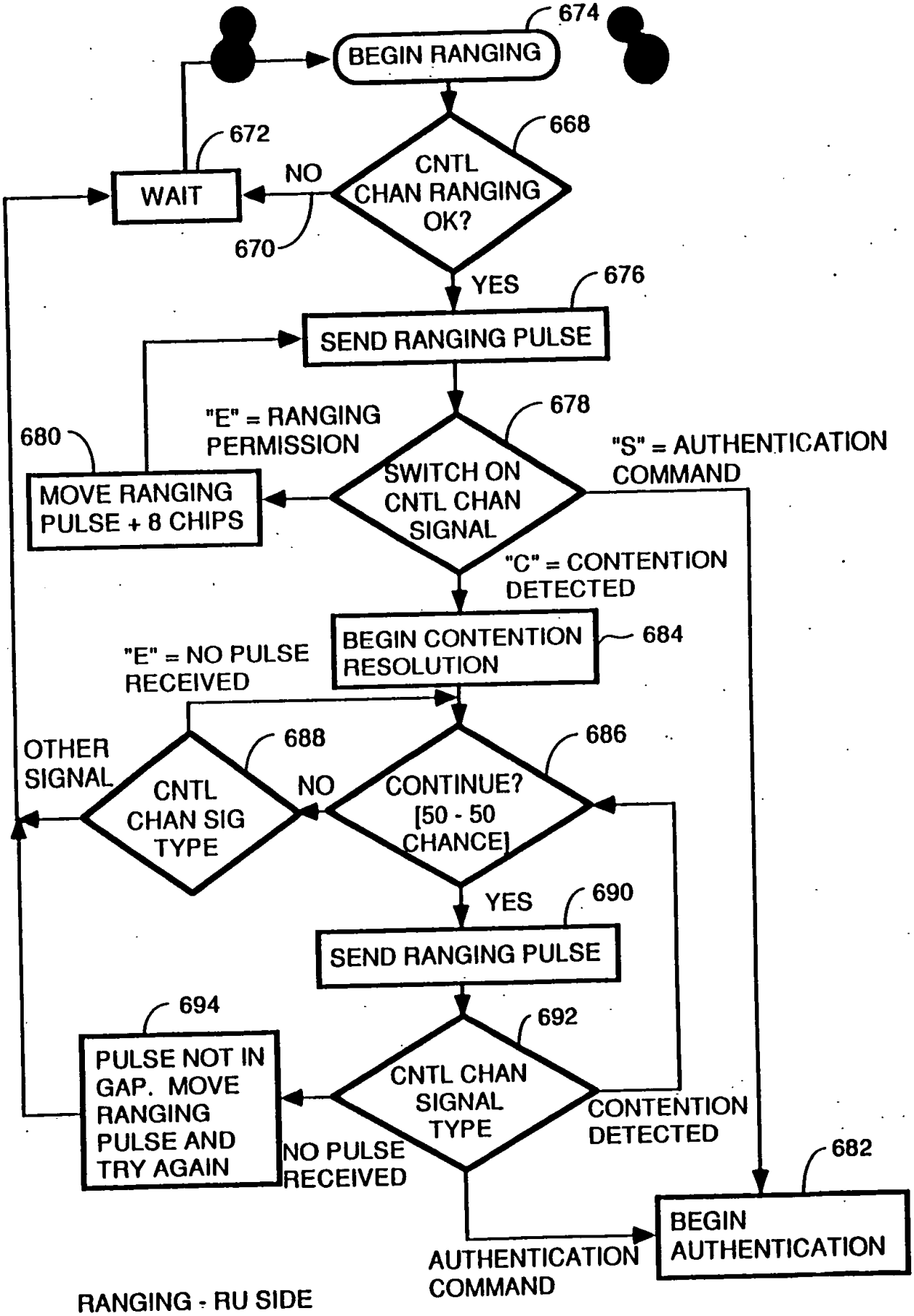
FIG. 31

41



CONTENTION RESOLUTION - RU USING BINARY STACK

FIG. 33



RANGING - RU SIDE BINARY TREE ALGORITHM

FIG. 32

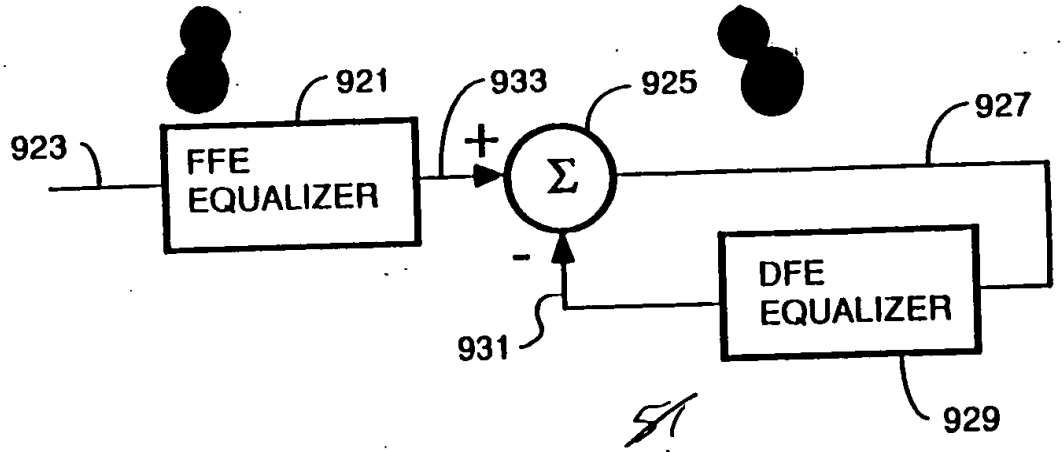


FIG. 37

50

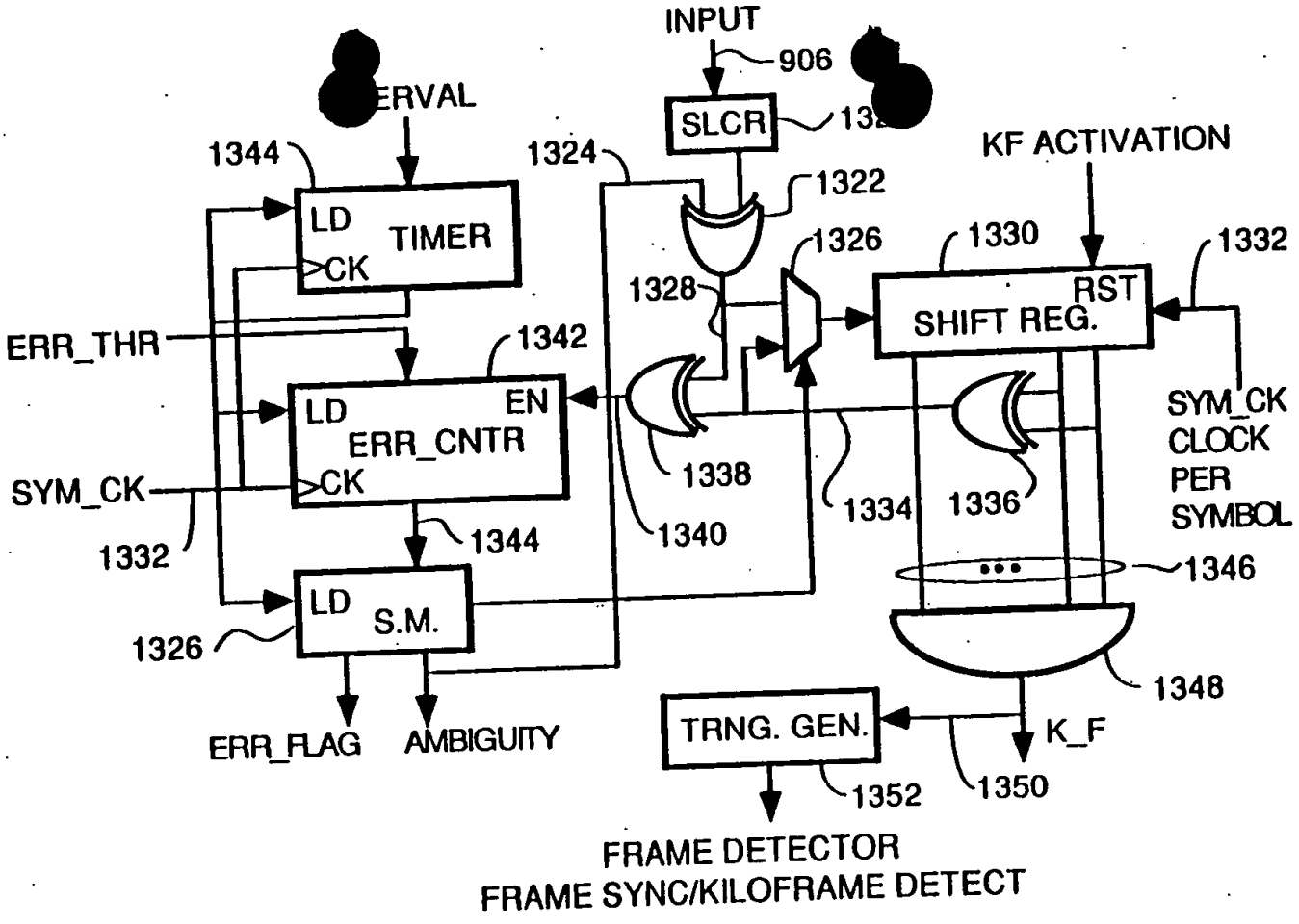
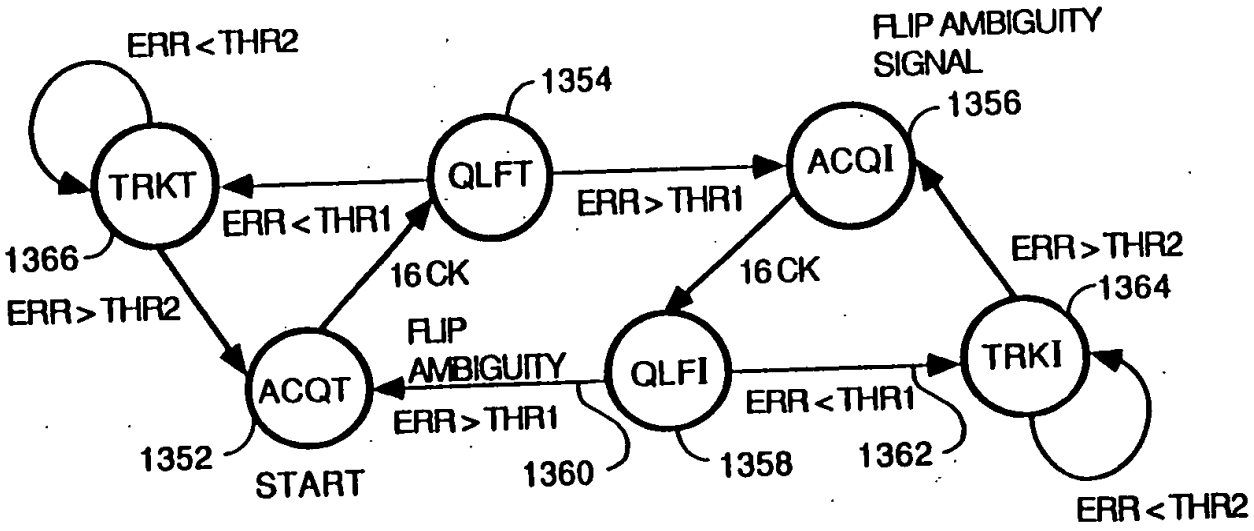


FIG. 52

51



STATE MACHINE

FIG. 53

52

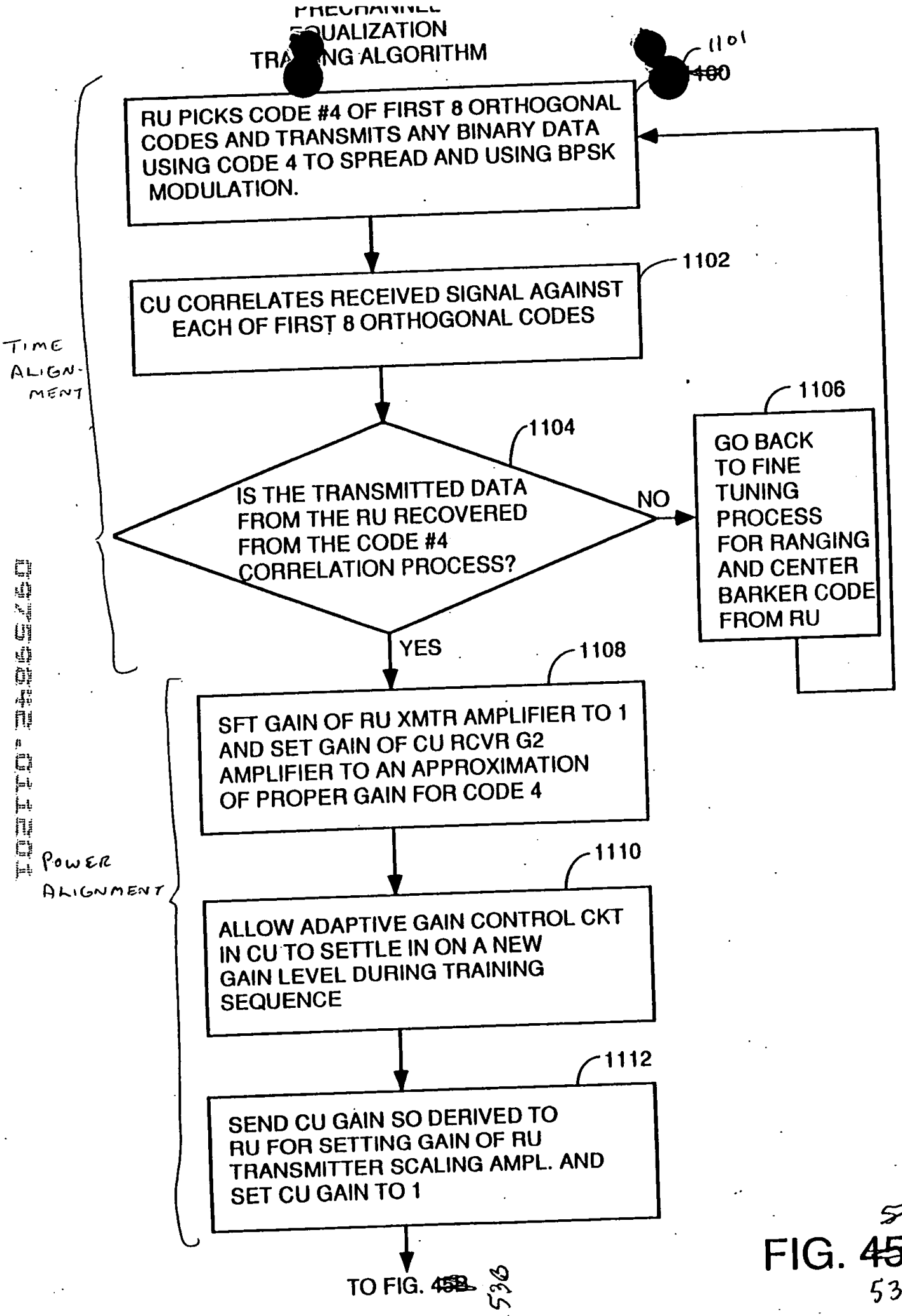

PRECHANNEL EQUALIZATION TRAINING ALGORITHM
1101
100
RU PICKS CODE #4 OF FIRST 8 ORTHOGONAL CODES AND TRANSMITS ANY BINARY DATA USING CODE 4 TO SPREAD AND USING BPSK MODULATION.
1102
CU CORRELATES RECEIVED SIGNAL AGAINST EACH OF FIRST 8 ORTHOGONAL CODES
TIME ALIGNMENT
1104
IS THE TRANSMITTED DATA FROM THE RU RECOVERED FROM THE CODE #4 CORRELATION PROCESS?
NO
1106
GO BACK TO FINE TUNING PROCESS FOR RANGING AND CENTER BARKER CODE FROM RU
YES
1108
SFT GAIN OF RU XMTR AMPLIFIER TO 1 AND SET GAIN OF CU RCVR G2 AMPLIFIER TO AN APPROXIMATION OF PROPER GAIN FOR CODE 4
POWER ALIGNMENT
1110
ALLOW ADAPTIVE GAIN CONTROL CKT IN CU TO SETTLE IN ON A NEW GAIN LEVEL DURING TRAINING SEQUENCE
1112
SEND CU GAIN SO DERIVED TO RU FOR SETTING GAIN OF RU TRANSMITTER SCALING AMPL. AND SET CU GAIN TO 1
TO FIG. 45B
53B

FIG. 45A

53A

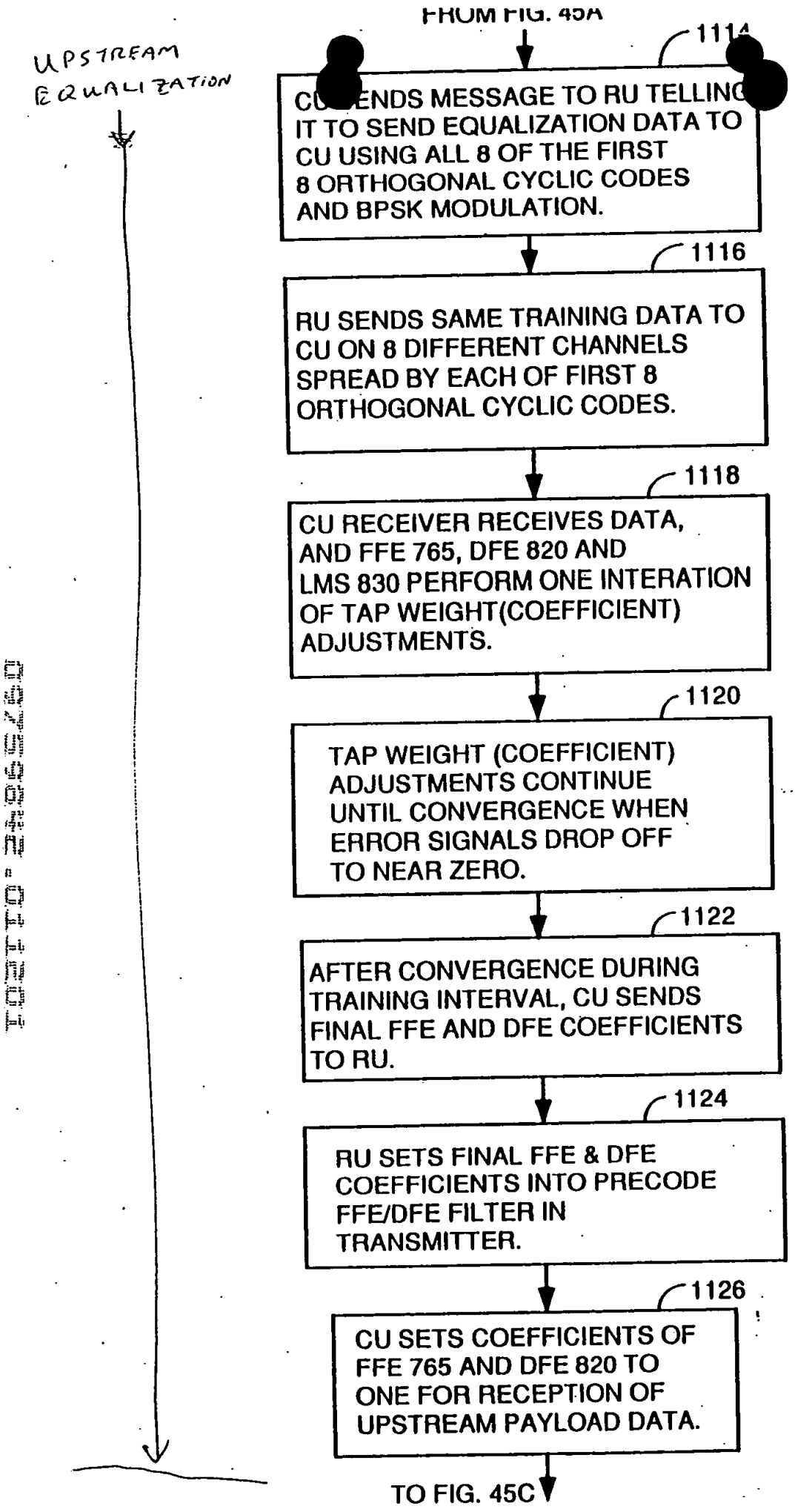


FIG. ~~45B~~ 54B 53B

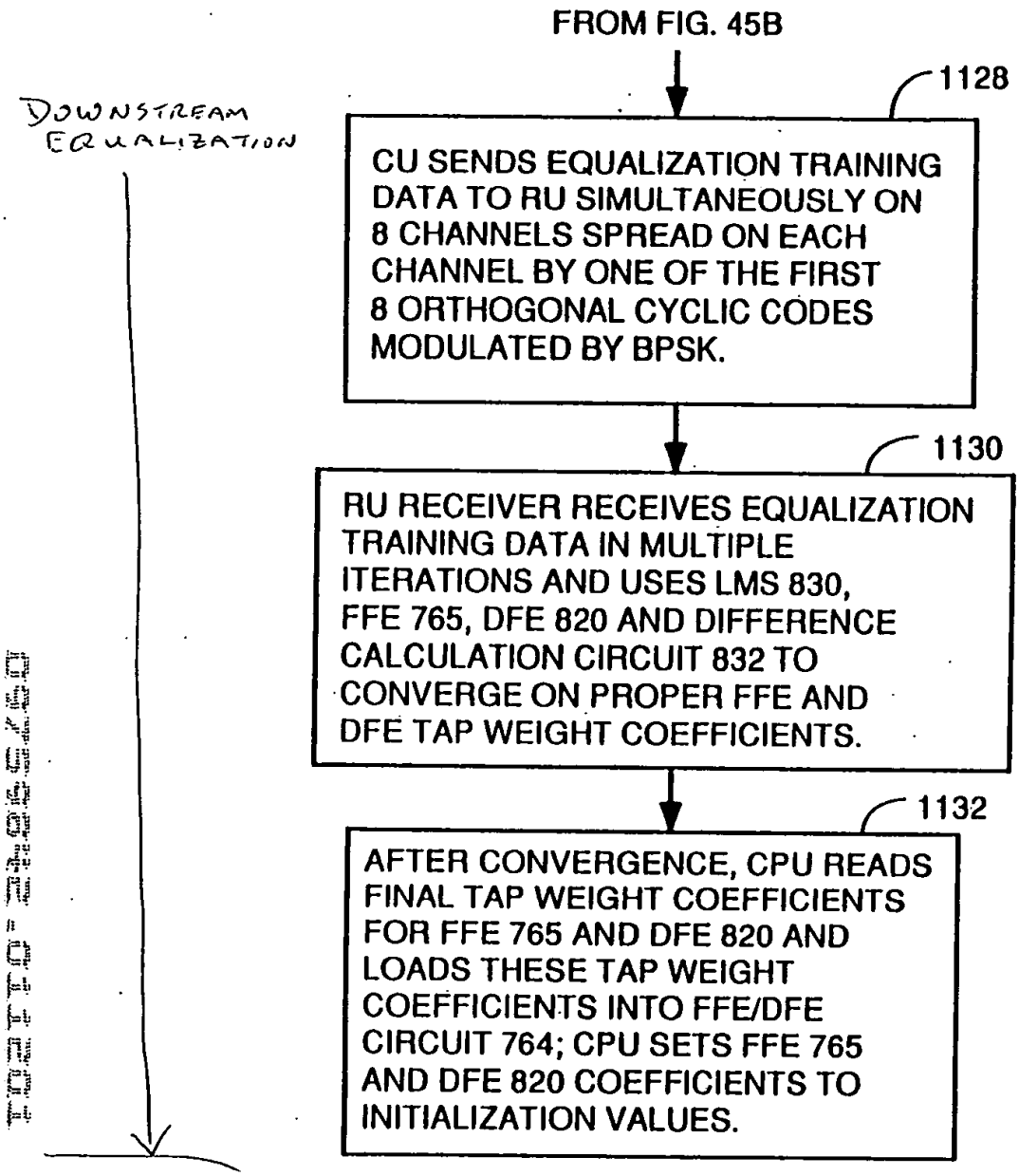

FROM FIG. 45B
DOWNSTREAM EQUALIZATION
1128
CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.
1130
RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.
1132
AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND LOADS THESE TAP WEIGHT COEFFICIENTS INTO FFE/DFE CIRCUIT 764; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

FIG. 45C

53C

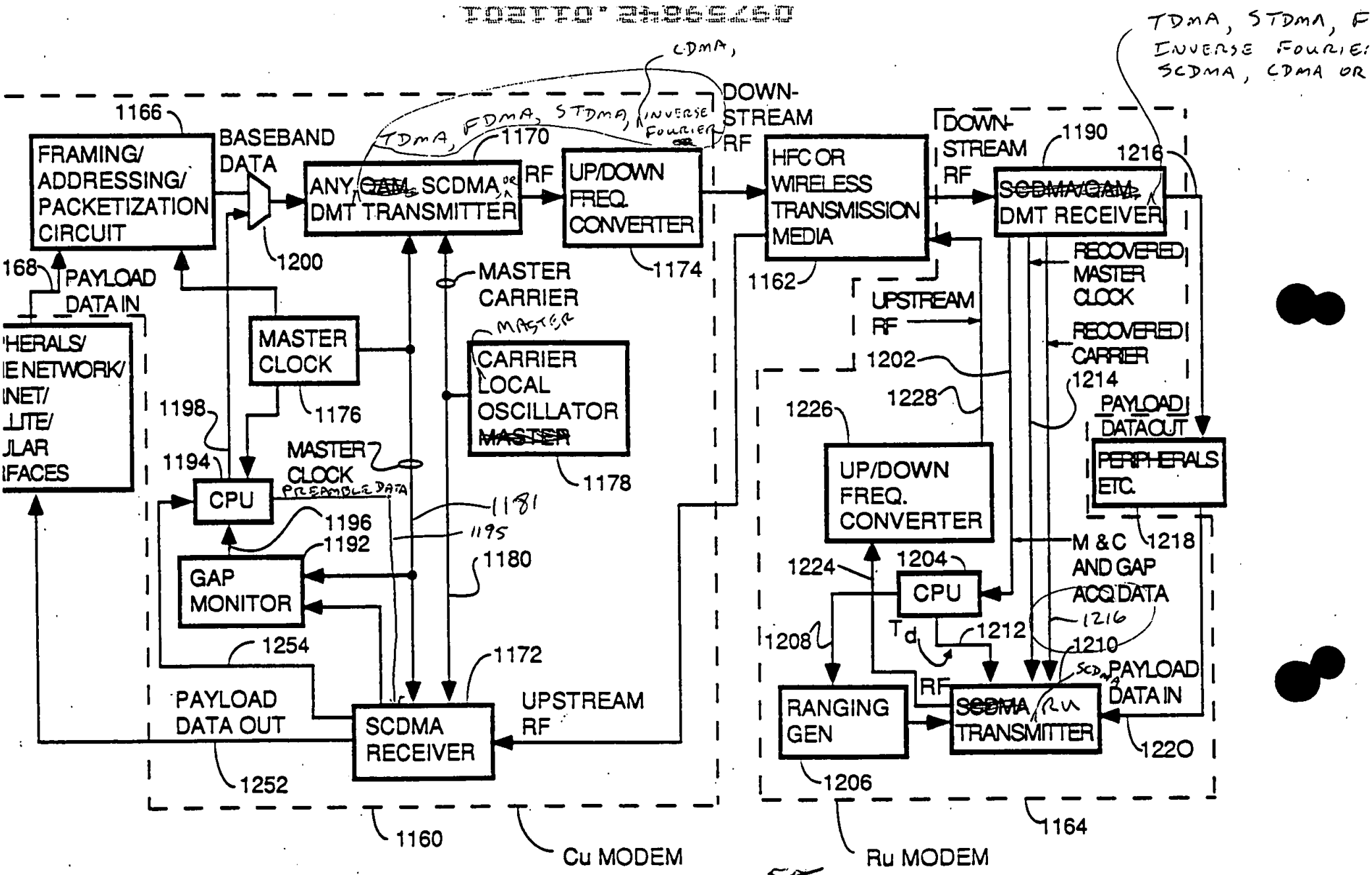
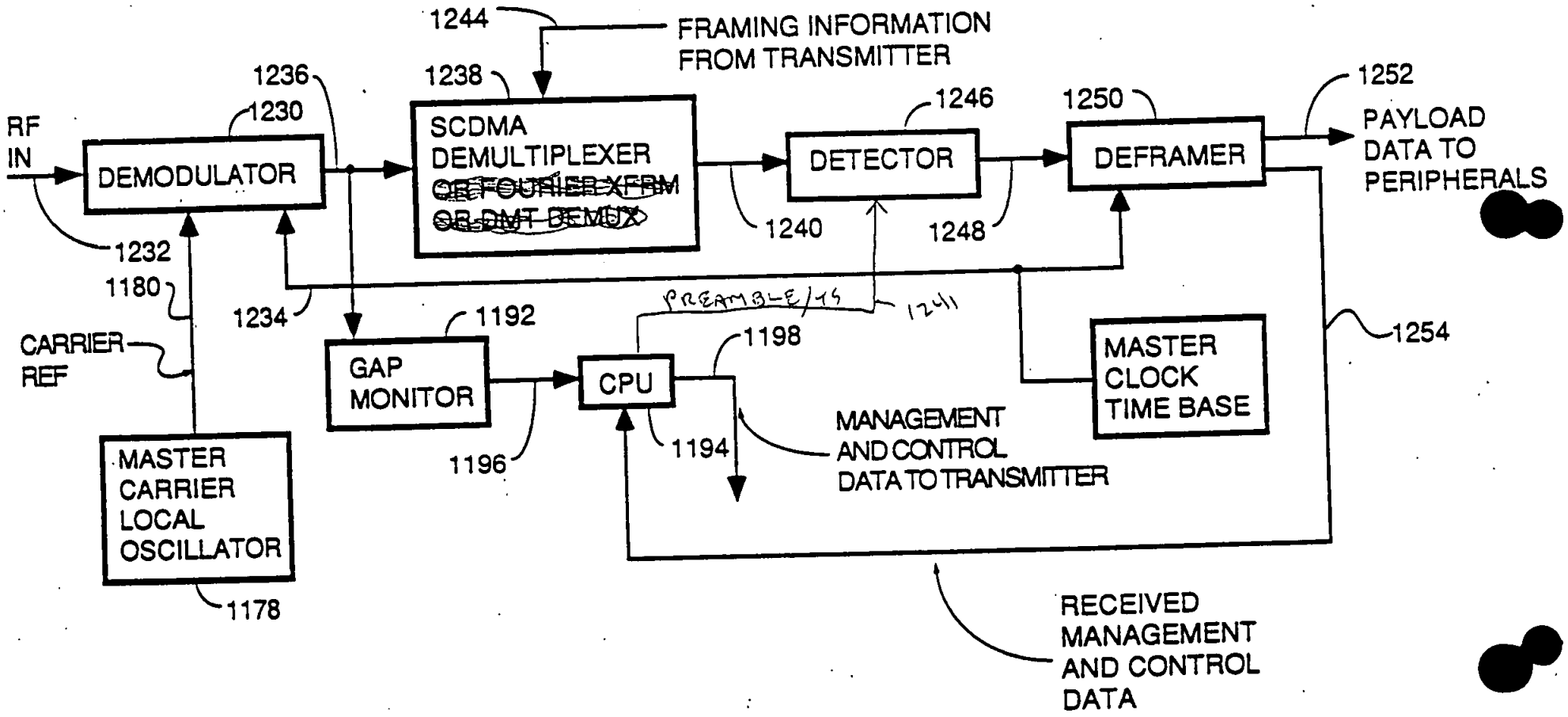

1166
FRAMING/ ADDRESSING/ PACKETIZATION CIRCUIT
BASEBAND DATA
1200
ANY, CDMA, SCDMA OR DMT TRANSMITTER
1170
RF
UP/DOWN FREQ. CONVERTER
1174
DOWN-STREAM RF
HFC OR WIRELESS TRANSMISSION MEDIA
1162
DOWN-STREAM RF
1190
1216
SCDMA/CDMA DMT RECEIVER
RECOVERED MASTER CLOCK
RECOVERED CARRIER
1214
PAYLOAD DATA OUT
PERIPHERALS ETC.
1218
168
PAYLOAD DATA IN
HERALS/ E NETWORK/ INET/ LITE/ JLAR FACES
MASTER CLOCK
1176
MASTER CARRIER
MASTER CARRIER LOCAL OSCILLATOR MASTER
1178
1198
1194
MASTER CLOCK
PREAMBLE DATA
CPU
1196
1192
1181
1195
1180
GAP MONITOR
1254
1172
PAYLOAD DATA OUT
SCDMA RECEIVER
UPSTREAM RF
1252
1160
Cu MODEM
UPSTREAM RF
1202
1228
1226
UP/DOWN FREQ. CONVERTER
1224
1204
CPU
M & C AND GAP ACQ DATA
1216
1208
Td
1212
1210
RF
PAYLOAD DATA IN
RANGING GEN
SCDMA TRANSMITTER
1220
1206
Ru MODEM
1164
TDMA, FDMA, STDMA, INVERSE FOURIER OR
CDMA,
TDMA, STDMA, F
INVERSE FOURIE
SCDMA, CDMA OR

FIG. 49

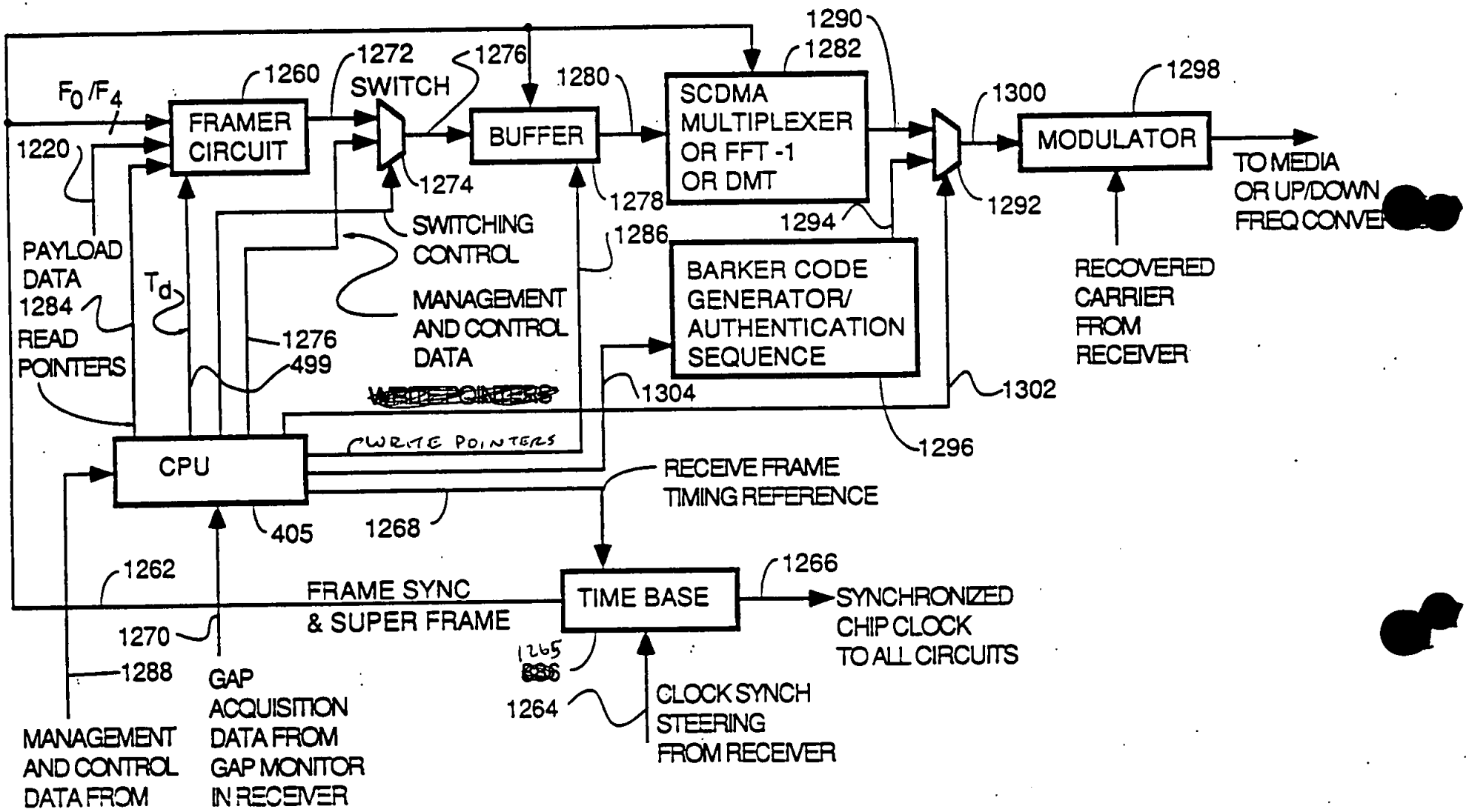
54



SIMPLE Cu SPREAD SPECTRUM RECEIVER

FIG. ~~50~~ 56

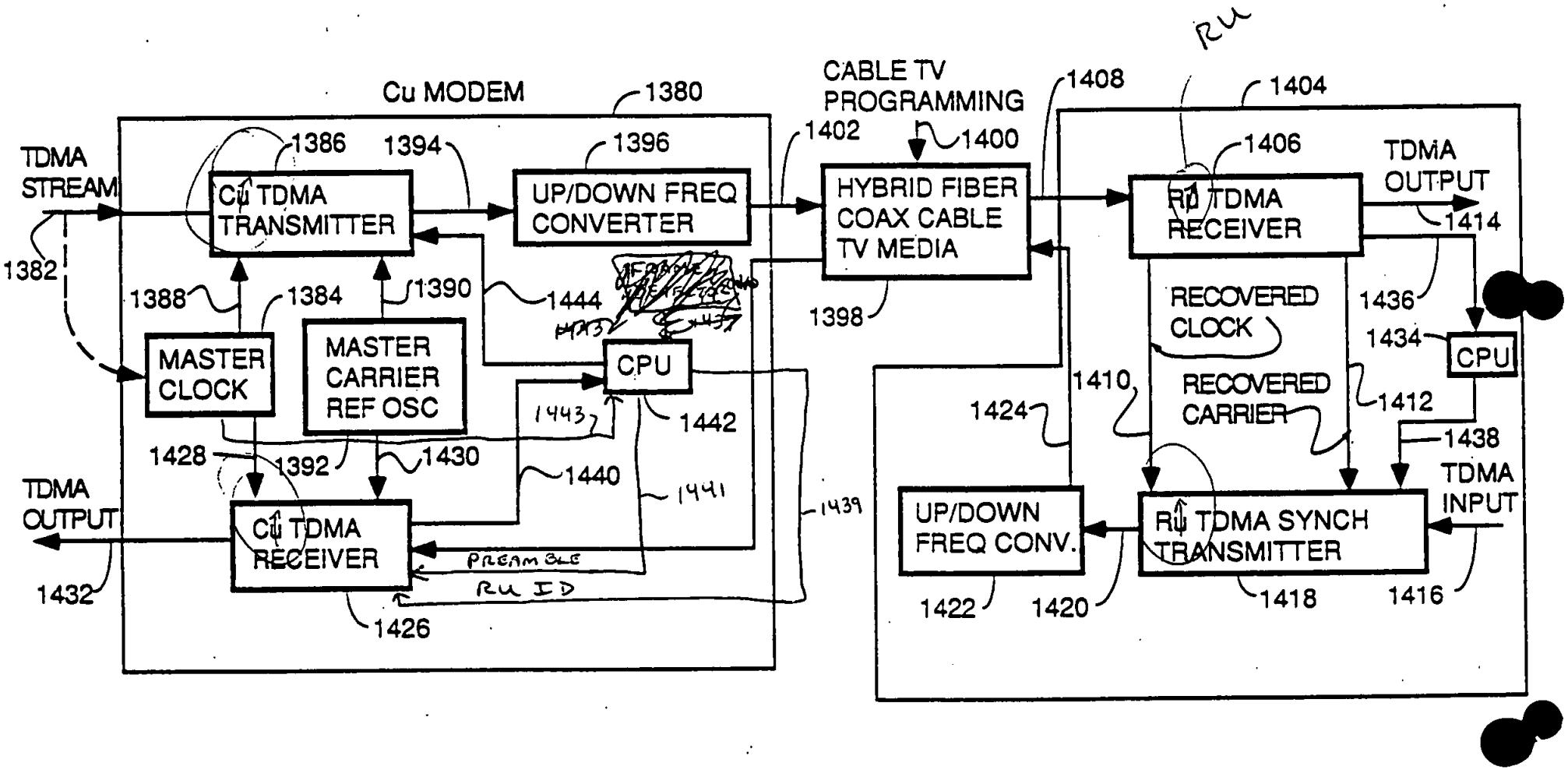
55



SIMPLE Ru SPREAD SPECTRUM TRANSMITTER

FIG. 51

56



SYNCHRONOUS TDMA SYSTEM

FIG. 54

57
57

OFFSET	1B ASIC		2A ASIC	
(Chips)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

Training Algorithm

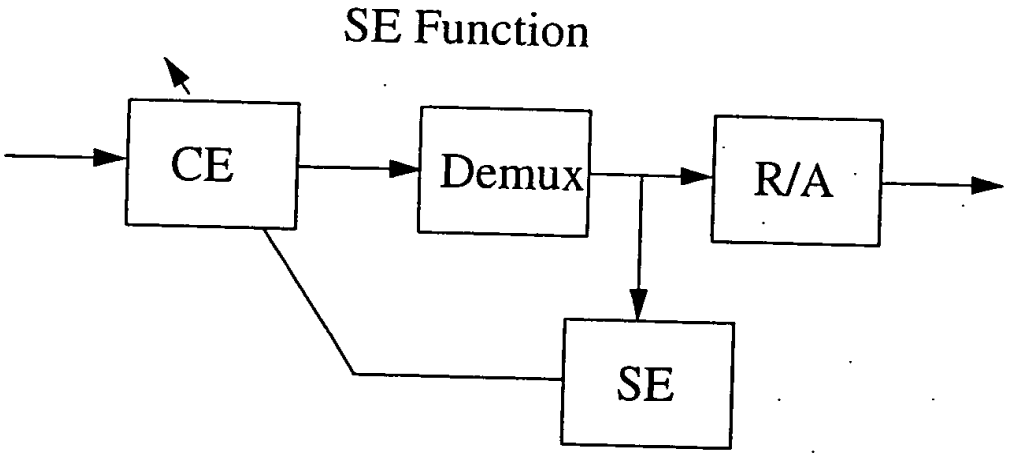
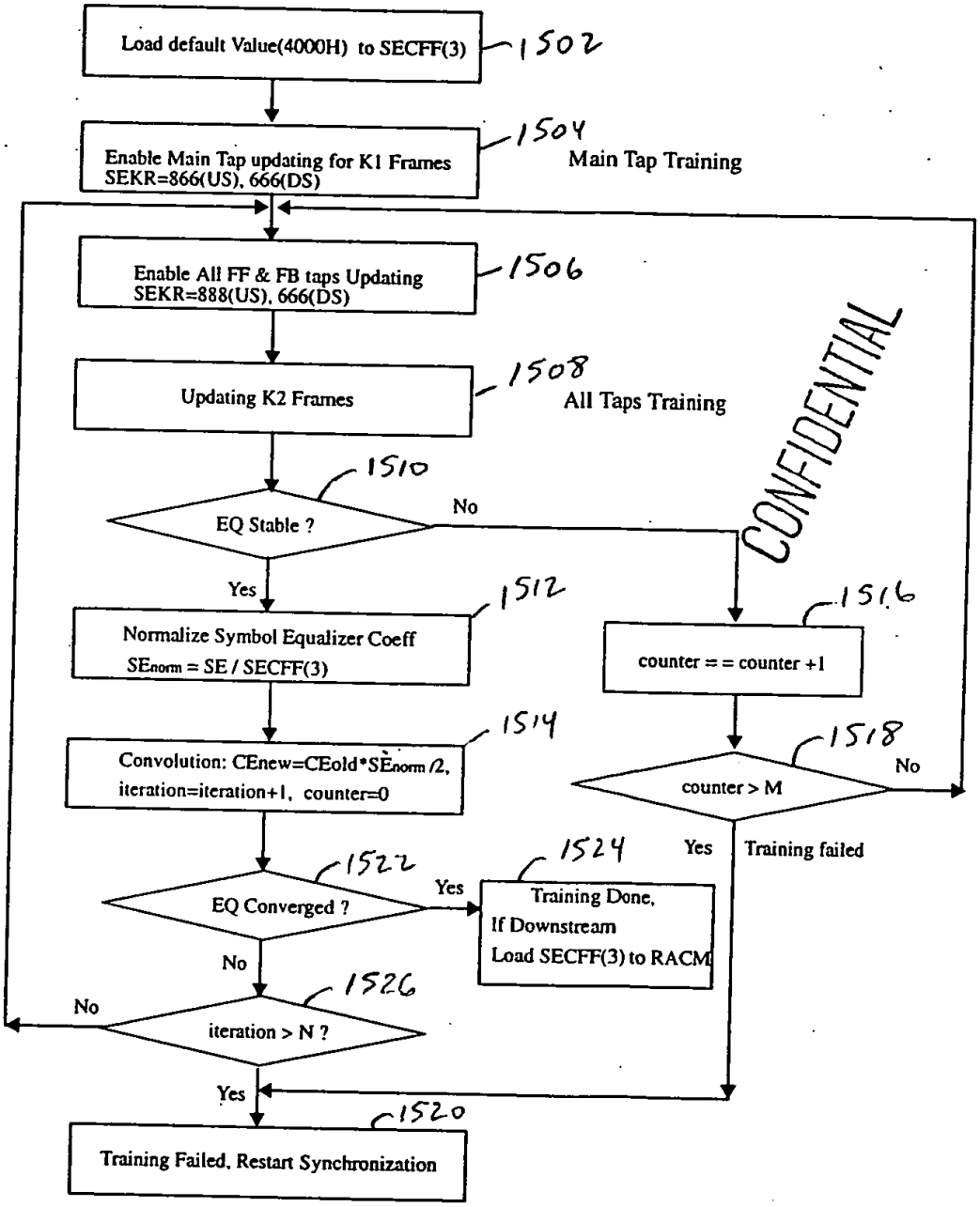


FIG. 59

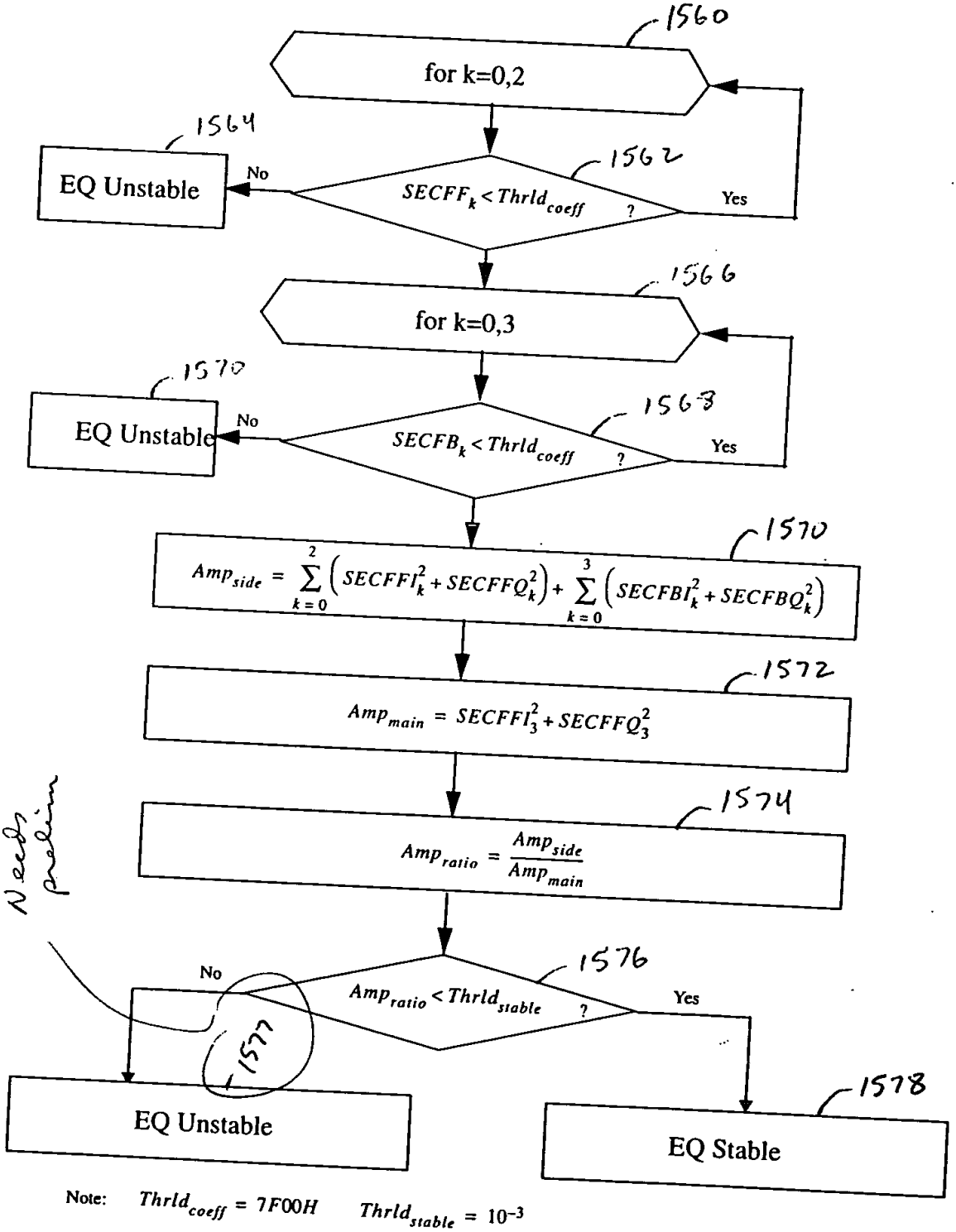
Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

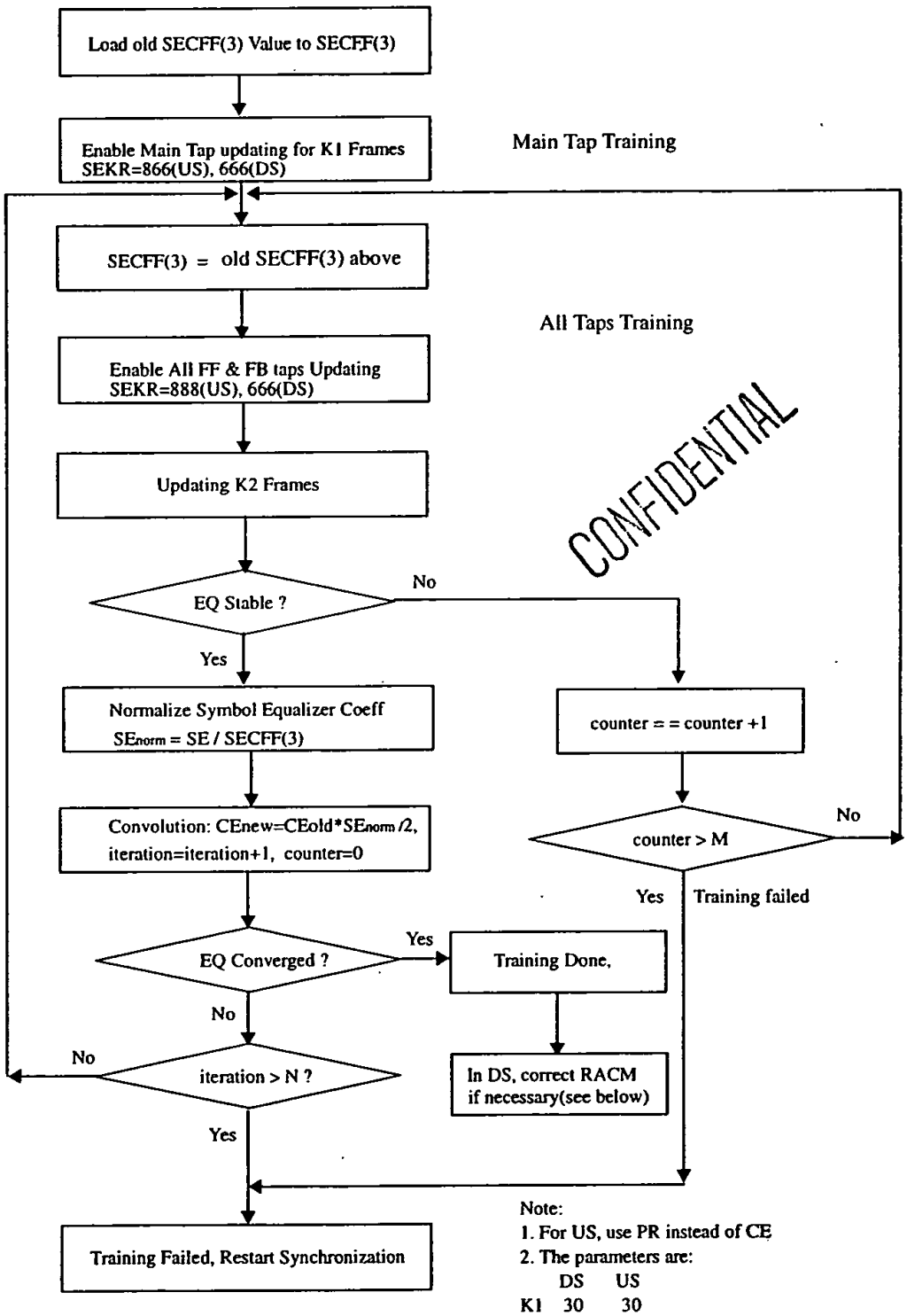
EQ Stability Check



Note: $Thrld_{coeff}$ = 7F00H $Thrld_{stable} = 10^{-3}$

FIG. 61

Periodic 2-Step Training Algorithm

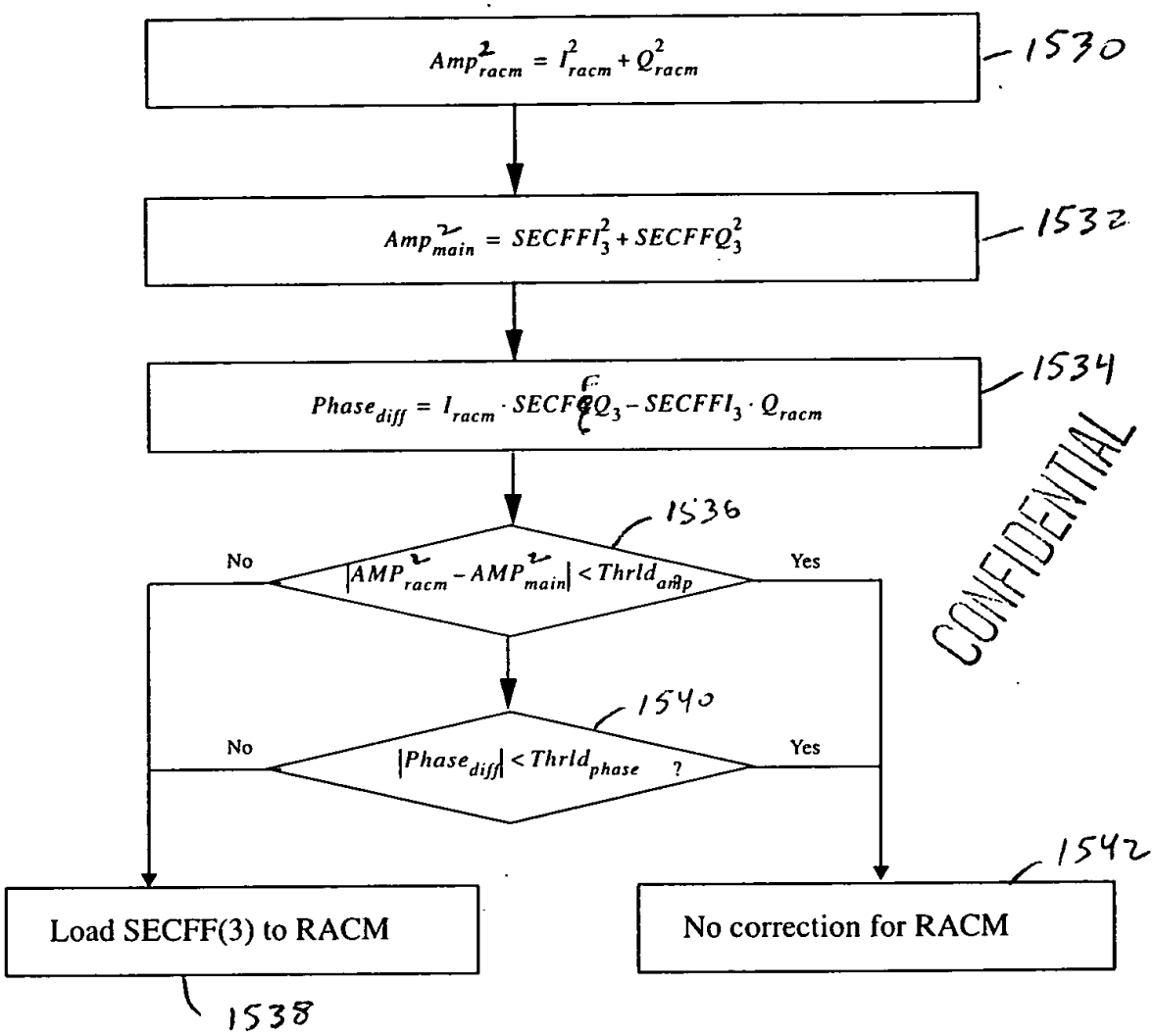


Note:
1. For US, use PR instead of CE
2. The parameters are:

	DS	US
K1	30	30
K2	20	30
N	5	3
M	3	3

FIG. 62

RACM Correction



CONFIDENTIAL

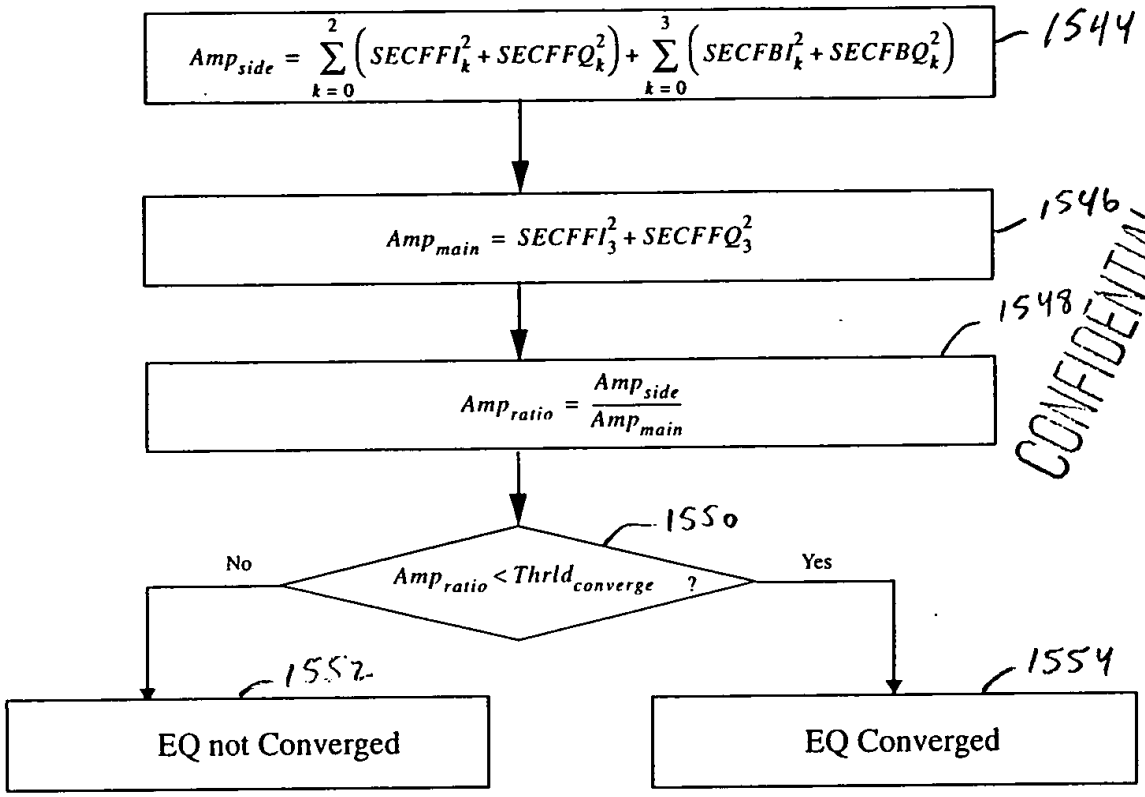
Note: $Thrld_{amp} = TBD$

$Thrld_{phase} = TBD$

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

EQ Convergence Check



Note: $Thrld_{converge} = 10^{-5}$

FIG. 64

Power Alignment Flow Chart

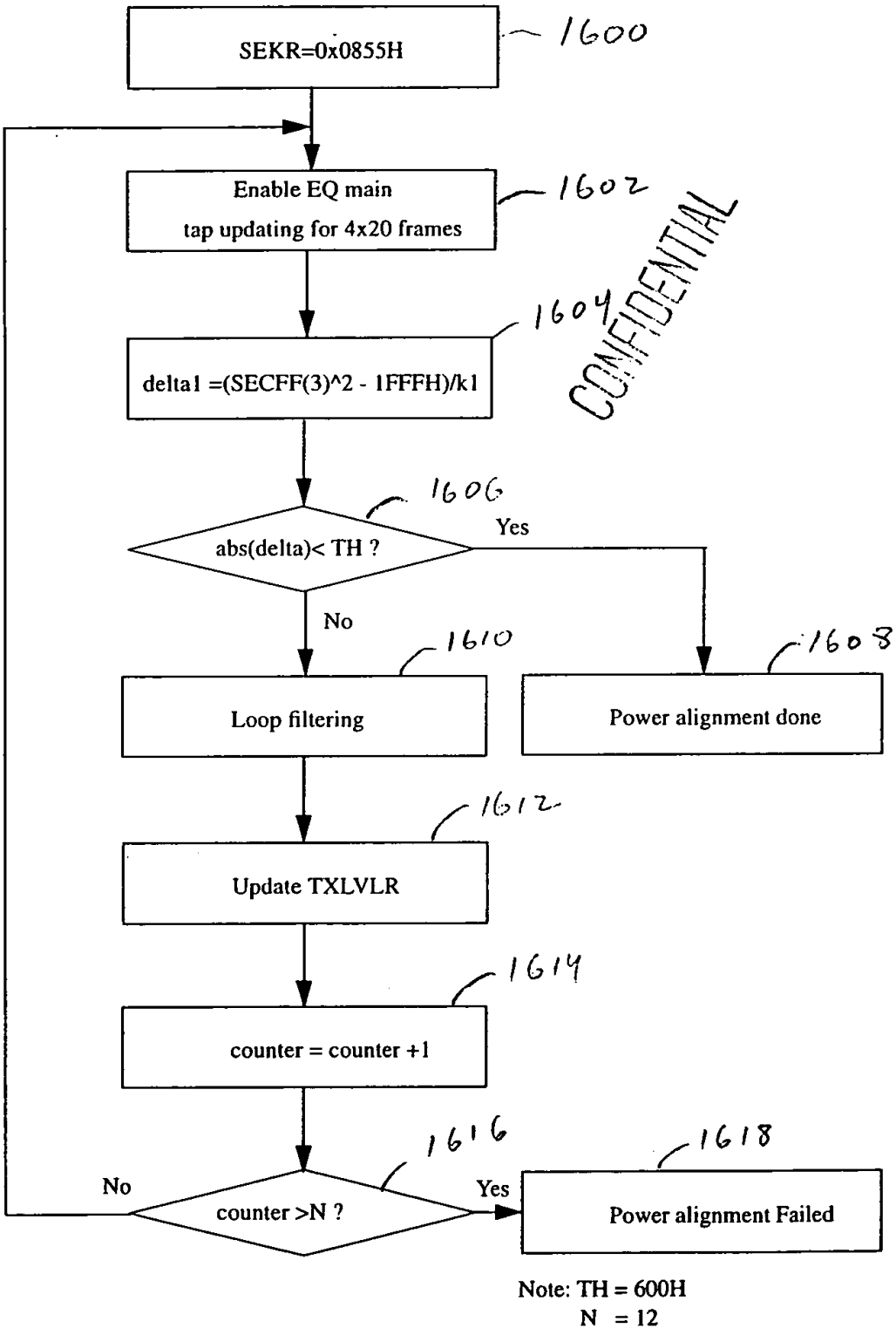


FIG. 65

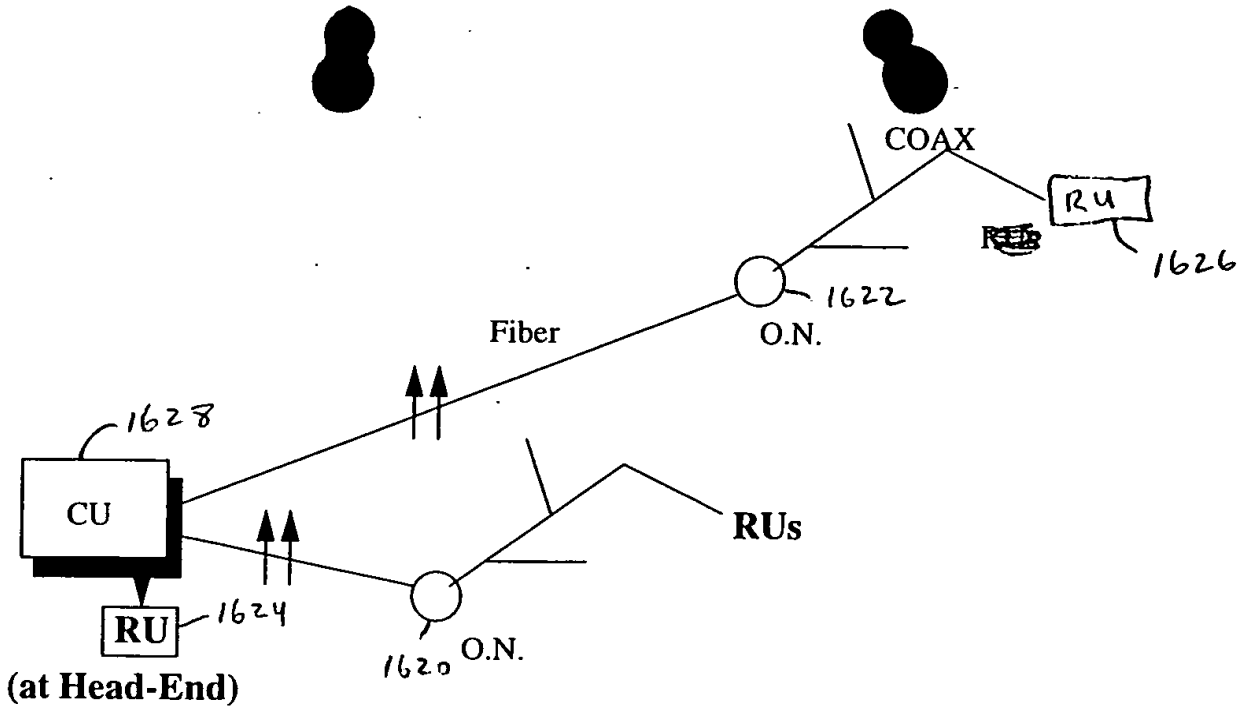
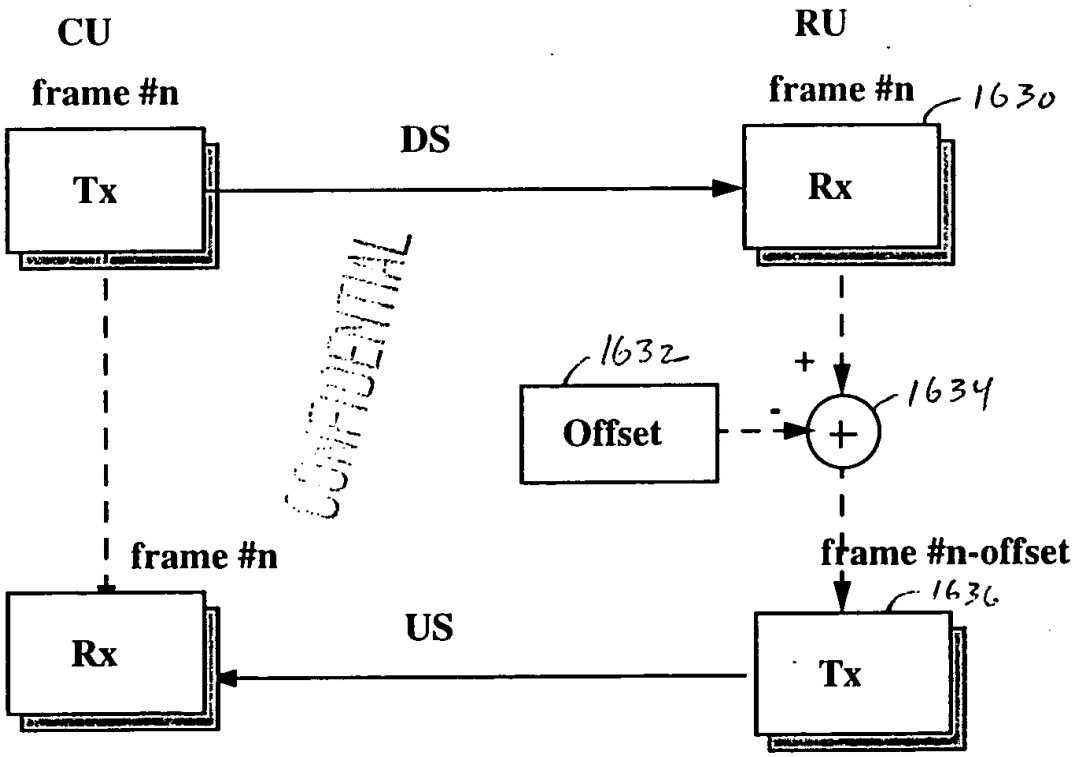


FIG. 66



Total Turn Around (TTA) in frames = Offset

FIG. 67

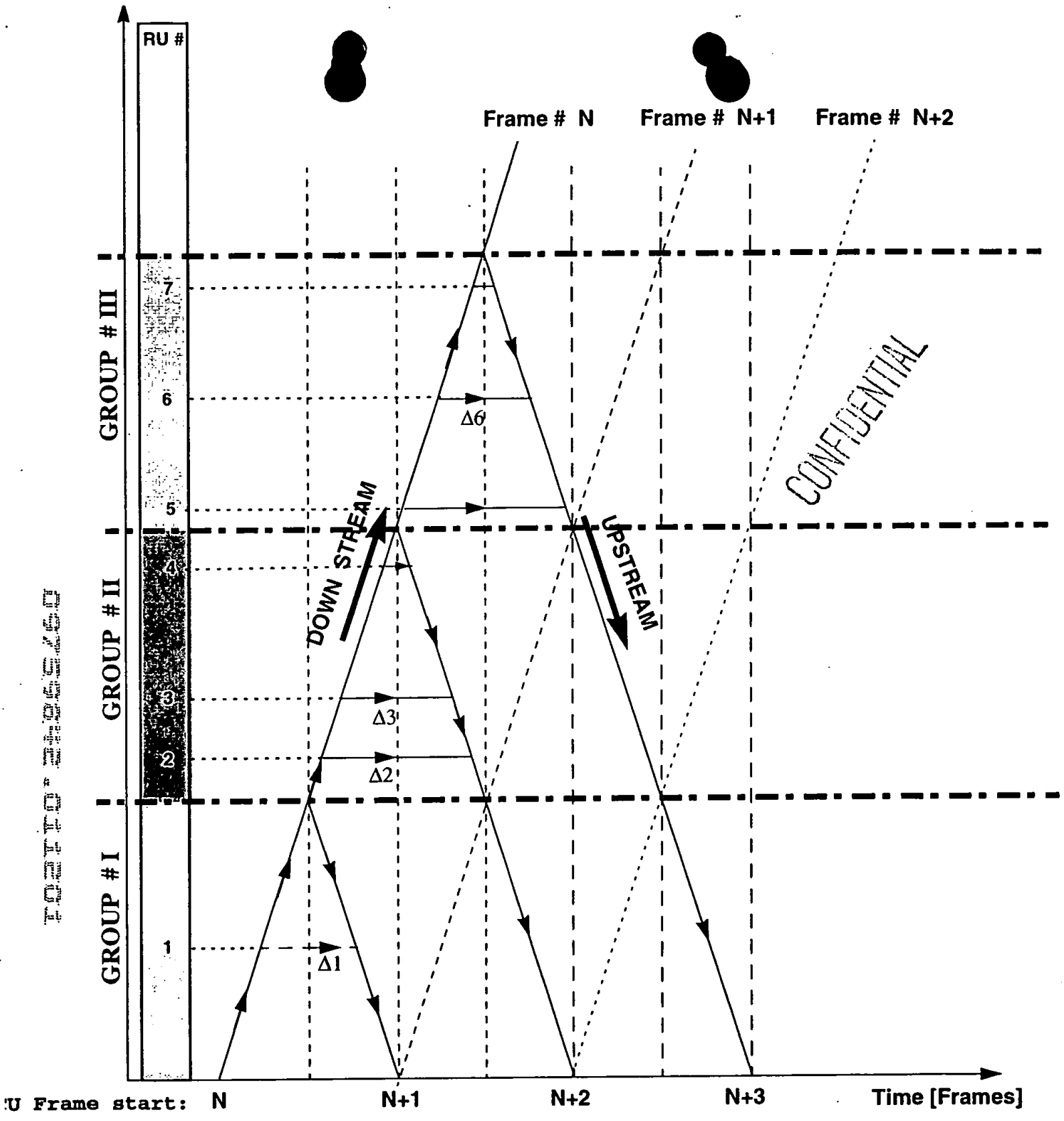


FIG. 6B

Figure 3.1: Frame start propagation along the channel

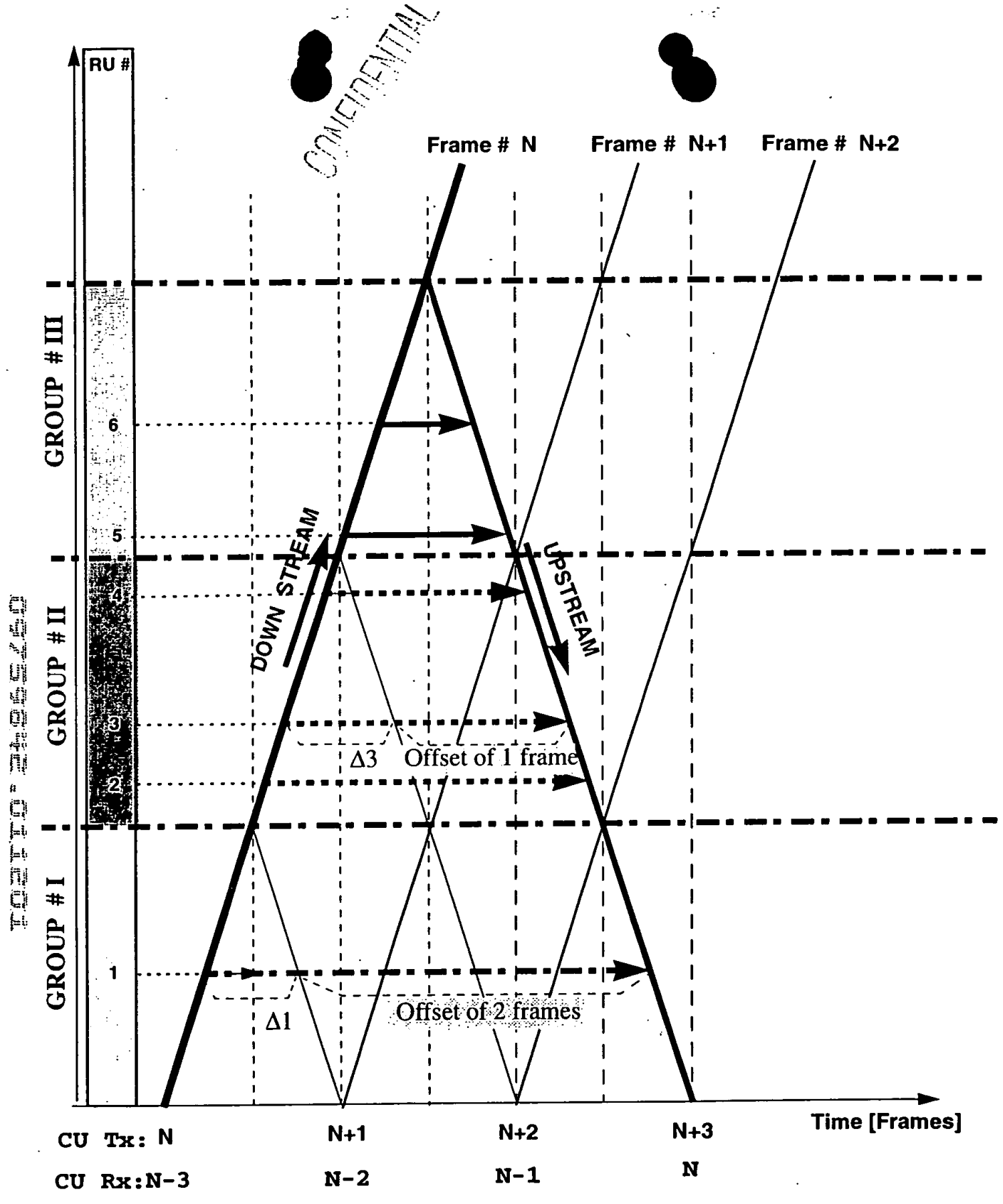


FIG. 69

Figure 69 Control message (downstream) and function (upstream) propagation in a 3 frames TTA channel

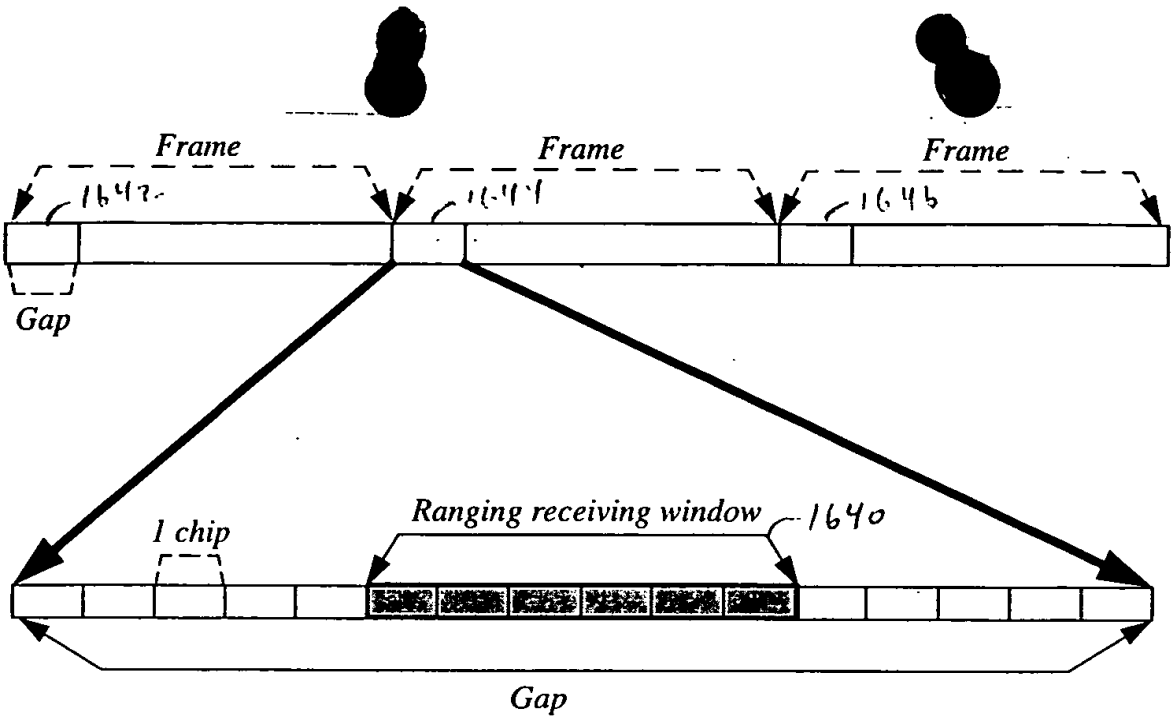

Frame
Frame
Frame
1642
1644
1646
Gap
1 chip
Ranging receiving window
1640
Gap

FIG. 7D

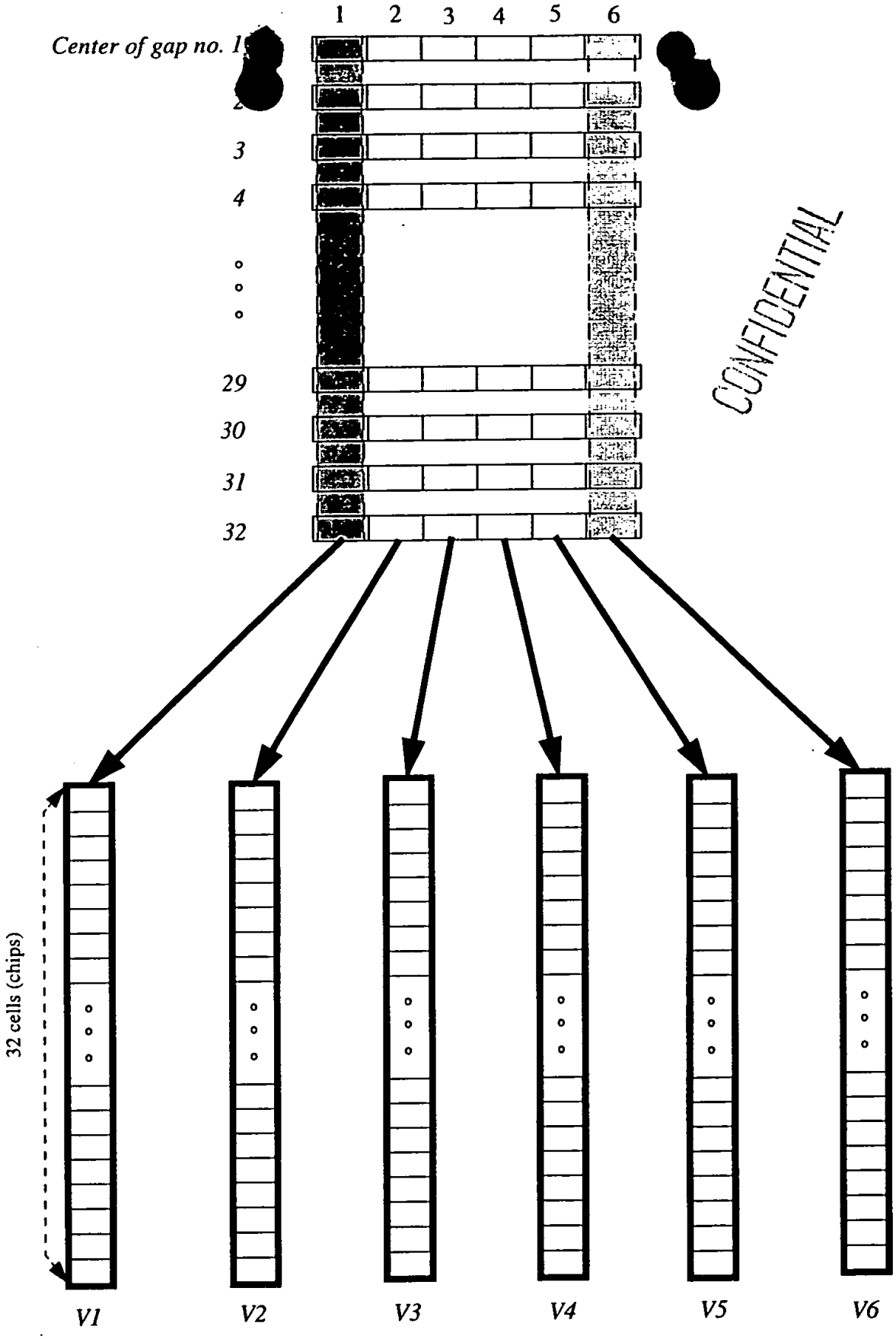


Figure 3.4: Overall view of the CU sensing windows in a "boundless ranging" algorithm

FIG. 71

Chip\FR	1	2	3	4	5	6	7		33
1	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**...**	**0**
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72